Wideband Dual-Injection Path Self-Interference Cancellation Architecture for Full-Duplex Transceivers

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Abstract—A transceiver front end including a dual-injection path self-interference (SI) cancellation architecture is proposed for use in wideband full-duplex networks. The SI cancellation circuitry is implemented using: 1) one feedforward cancellation path containing a five-tap analog adaptive finite-impulse response (FIR) filter between the transmitter (TX) output and the receiver (RX) input; 2) a second baseband (BB) cancellation path containing a 14-tap low-frequency FIR filter with a point of injection at the RX BB output; 3) a phase noise cancellation method that suppresses the reciprocal mixing products associated with the downconversion in the BB cancellation path for the TX SI signal; and 4) an integrated noise cancelling power amplifier (PA). A prototype of 40-nm TSMC device was fabricated, which demonstrates more than 50-dB SI cancellation over 42-MHz bandwidth and a 10-dB attenuation of TX SI phase noise in the RX signal path. The two cancelling filters dissipate 11.5 mW, with a measured $P_{-1\,dB}$ and IIP_3 of 27/26.5 and 36/34.5 dBm, respectively. The RX noise figure is degraded by less than 1.55 dB, when both cancellers are enabled. The PA has a measured output of $P_{-1\,dB}/P_{sat}$ of 25.1/26.5 dBm, respectively. The total chip die area is 3.5 mm^2 with an overall transceiver power consumption of 49 mW, excluding the integrated PA.

Index Terms—Adaptive finite-impulse response (FIR) filters, CMOS integrated circuits, delay lines, fifth generation (5G) mobile communication, interference cancellation, radio frequency, radio spectrum management.

I. Introduction

THE demands for higher wireless data rates continue to remain strong with some estimates projecting a factor of 5–10× increase in the upcoming years. This is driven by applications, such as video delivery to mobile smartphones, cloud computing, and the Internet-of-Things (IoT) [1]–[4]. However, all of the spectra below 6 GHz are allocated to the existing standards and applications, such as ZigBee, GPS, cellular phones, and Wi-Fi networks, in addition to frequency allocations dedicated to government functions including police, fire, and military communication. Full-duplex (FD)

communication presents an opportunity to increase spectral efficiency by allowing a single radio's transmitter (TX) and receiver (RX) to simultaneously operate using one carrier frequency (on the same channel) [5]–[19], for better usage of the existing commercial radio spectrum and effectively increasing the capacity of the existing wireless networks.

Although FD communication will potentially increase spectral efficiency by as much as 2× when compared to the existing frequency division duplex (FDD) systems, significant engineering challenges, which includes the cancellation of the TX self-interference (SI) signal present at the RX front-end [5]–[7], [20]–[34], exist. The large difference between the maximum TX power and the minimum required RX sensitivity demands a method to attenuate the signal power of the strong TX SI signal, which is particularly true in high-performance applications such as Wi-Fi, cellular, and evolving fifth generation (5G) wireless standards. As an example, some flavors of Wi-Fi transmit up to +20 dBm output power, while the RX sensitivity is as low as −90 dBm. Depending on the modulation method, more than 120 dB SI cancellation may be required [Fig. 1(a)].

To achieve a high SI cancellation (∼120 dB) compatible with longer range radios that require a high output power TX, the function of SI cancellation should be distributed along the RX chain. For example, using an air interface that is realized with either a single antenna and a circulator, or two antennas, and assuming that these components provide a TX–RX isolation up to 30 dB, and further assuming that a 40 dB cancellation is provided by the digital backend, this leaves approximately 50 dB of cancellation for the analog/RF front end to achieve [see Fig. 1(b)] [23].

An ideal SI canceller should contribute minimal noise to the RX front end, occupies minimal silicon area, and has minimal added power consumption [35]. There have been numerous recent efforts to perform on-chip SI cancellation in the analog/RF front end. These cancellation techniques can be categorized as either passive [35]–[47] or active methods [21]–[24], [31], [48]–[57]. However, these methods often occupy significant silicon die area [35]–[47] or provide insufficient canceller linearity performance, which limits the maximum TX output power [21]–[24], [31], [48]–[57]. Moreover, both the depth and bandwidth (BW) of the cancellation are insufficient for applications that operate on a wide BW (>40 MHz), multi-carrier, high-output power amplifier (PA)
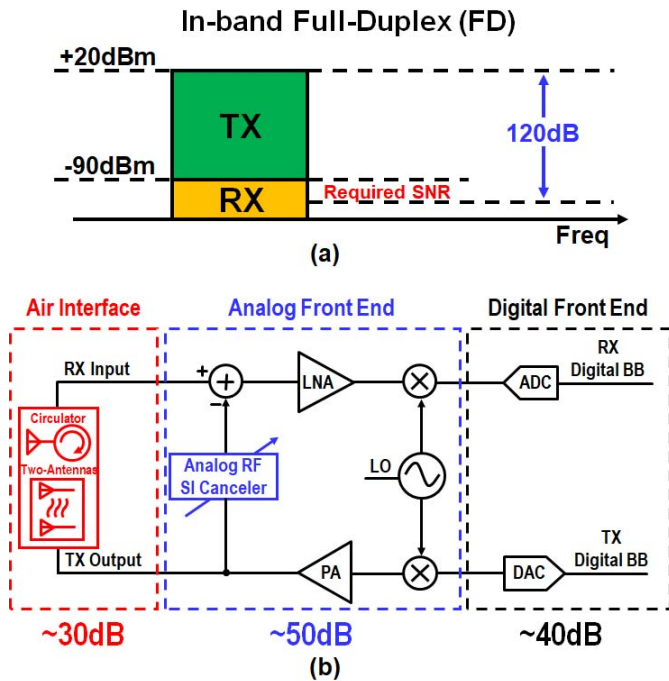
Fig. 1. SI cancellation in FD communication. (a) SI cancellation requirement in an FD radio with a TX output power of 20 dBm and a RX-required sensitivity of −90 dBm. (b) SI cancellation distributed in the RX chain.
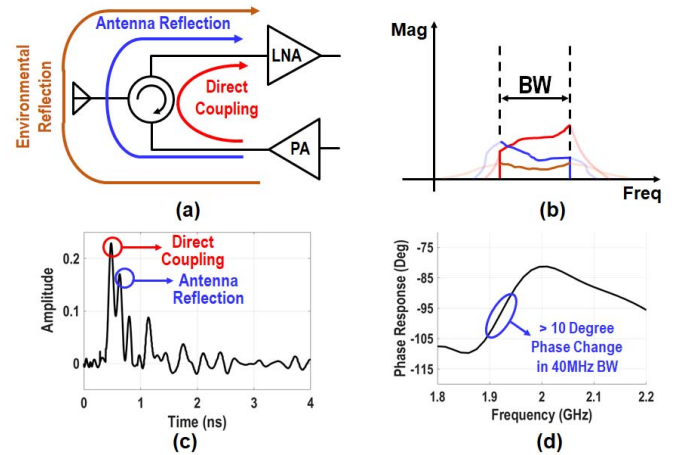

Fig. 2. Channel response of the leakage path. (a) Multiple time delay paths of the leakage signal coupled from PA output to LNA input. (b) Conceptual frequency response for each time delay versions of the leakage signal. (c) Impulse response of a discrete circulator from Meca Electronics. (d) Phase response of the measured discrete circulator.

signal, as is the case with evolving 5G wireless standards. Thus, the focus of the FD front end described in this paper is on the realization of a cancellation network that operates on a broad channel BW (40 MHz), with deep SI attenuation (50 dB+) as well as high linearity to allow the integration of high-output power PA ($P_{sat} = 25$ dBm and $P_{max} = 15$ dBm in the FD mode).

The design of a high-performance wideband SI canceller is challenging due to the fact that there are multiple time delayed paths of the SI signal over the channel BW of interest. A transceiver front end with a circulator and a single TX/RX shared antenna is used to illustrate this concept [Fig. 2(a)]. The SI is a combination of several leakage paths that include: 1) a direct-coupling path through the circulator, chip, and board substrate; 2) reflection from the antenna due to the imperfect matching between the antenna and the RX; and 3) a combination of other environmental reflections from nearby objects (e.g., human ear and metal objects). Each of the SI leakage paths will have a different frequency response and transfer function [Fig. 2(b)]. If it is assumed that each leakage path is linear time-invariant (LTI), then the overall leakage channel response can be modeled as a combination of the frequency response associated with each leakage path. To better understand the existence of multiple time-delayed coupling paths between the TX and the RX, measurements were made of a commonly found discrete circulator (Meca Electronics #CS-1.950) using a network analyzer and the results of which are shown in Fig. 2(c) and (d). This indoor measurement was taken with the antenna port of the circulator terminated using a 50-Ω load impedance. A two-port

short-open-load-through (SOLT) calibration is performed on the TX and RX ports before taking the actual circulator measurement. It is worth mentioning that the measured circulator response is different from the actual leakage channel response. The leakage channel response is complicated and should take into account some secondary effects such as the response of the cable and package. The measured phase response of the circulator from the TX to the RX port shows a significant change (10°) over a BW of 40 MHz due to the multiple time-delayed coupling paths [see Fig. 2(d)]. As such, to realize a wideband suppression of the TX-to-RX SI, the canceller must provide an inverse channel response of all the summed leakage paths.

Several recent research efforts attempt to achieve wideband and high SI cancellation using a single feed-forward path [21] or a single point of injection [51]. In [21], a second-order G_m-C N-path filter was used to perform frequency domain equalization. However, a high-frequency multiphase clock network must be distributed to a set of switches, which will likely dissipate considerable power. An alternative method synthesizes an inverse leakage signal at the LNA input using a current DAC and upconversion mixer [51]. However, for applications requiring a high RX sensitivity, the DAC quantization noise will potentially degrade the RX sensitivity. Thus, it is challenging to achieve sufficient SI suppression using a single feedforward path for a wideband TX signal, in situations where a high-power PA operates simultaneously with a high-sensitivity RX. Moreover, the cancellation DAC lacks the ability to capture the broadband noise and non-linearities produced by the TX. While examples do exist of a single-circuit block achieving TX SI cancellation of greater than 50 dB [39] for narrowband applications, generally achieving this level of suppression/cancellation for a wideband signal remains difficult. Examples might include single-sideband mixers [58], filters, and harmonic rejection mixers [59], [60].
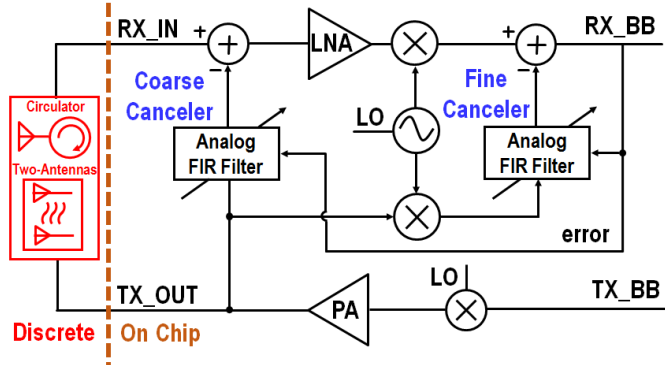
Fig. 3.   Proposed dual-injection path SI cancelling architecture.

Fig. 4.   RF canceller (analog FIR filter) block diagram.

The remainder of this paper explores an SI cancelling architecture that overcomes those aforementioned challenges by performing SI cancellation at multiple points in the RX. This is followed by an expanded description of the prototype chip, which was first given in [20].

II. Dual-Injection Path Full Duplex Architecture

This transceiver makes use of a dual-injection path SI cancelling architecture that allows more design freedom to achieve both a deeper attenuation of TX leakage over a broader BW (see Fig. 3). Two analog cancellers, both of which have their inputs attached to the TX output matching network, are designed to properly capture not only the TX carrier signal, but also the noise and non-linear distortion introduced by the TX.

The first RF canceller resides between the PA output and the RX LNA input, with the primary function of reducing the TX SI power sufficiently to prevent the RX front end from saturating. This has the effect of relaxing the required linearity for the LNA and all the subsequent RX blocks. The second baseband (BB) canceller benefits from the RX gain (30 dB), and thus, the RX is more forgiving of a noisy feedforward injection path as compared to a canceller with an output that feeds the RX input. This allows the realization of a significantly lower frequency, complex I/Q 14-tap analog finite-impulse response FIR filter. The BB canceller has an added advantage of capturing and cancelling the TX leakage reciprocal mixing with the LO phase noise in the RX signal path. The combination of both cancelling filters, with their outputs injected at different points in the RX chain, provides a wideband and high SI cancellation. More details covering the design of this dual-injection point cancelling architecture are discussed in Section III.

III. Dual-Injection Path Canceller Design Considerations

Several practical design issues are associated with this FD architecture, which include: 1) system-level design tradeoffs between the cancellation BW and the noise performance; 2) canceller design techniques to improve the linearity; and 3) cancellation of the TX SI signal reciprocal mixing with the LO phase noise in the second BB cancellation path.
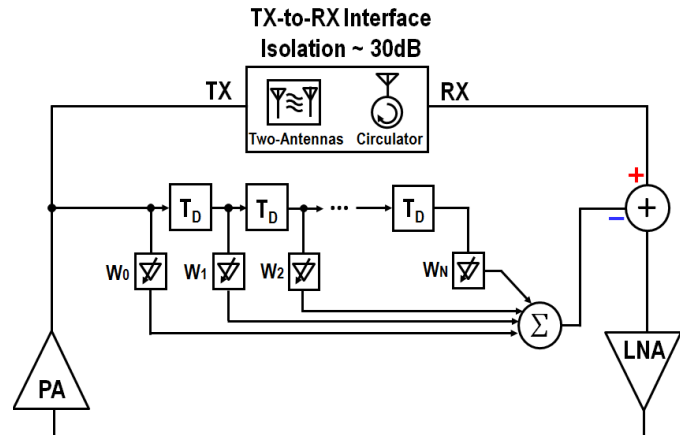
A. First Coarse RF Canceller

The RF cancellation path is implemented with an analog adaptive FIR filter using true-time delay blocks for the delay elements and transconductance stages to realize the filter taps [61] (Fig. 4). A similar approach to an RF feedforward canceller was demonstrated in the discrete form at Sigcomm [5]. As mentioned earlier, the RF canceller is designed to attenuate the TX SI signal significantly, thus relaxing the linearity requirements of the entire RX. However, there exist design tradeoffs between the number of filter taps used by the feedforward canceller, the degradation in the RX noise figure due to the noise generated by the canceller path, and the cancellation bandwidth (BW). To better understand these tradeoffs, a set of simulations were performed with both MATLAB Simulink (cancellation BW simulation) and Cadence SpectreRF (noise simulation); results are given in Fig. 5. In the MATLAB simulation, the all-pass filter (APF) stages were kept ideal and implemented using transfer function, while in the Cadence noise simulation, actual circuit components were used. The noise figure degradation plots highlighted in Fig. 5 were based on the Cadence SpetreRF simulations, assuming a 4-dB baseline RX NF. These simulations were also performed with each tap consuming the same power and contributing the identical amount of noise to the RX signal path.

The tap delay line is modeled as a first-order APF with a transfer function, which is given as [61]

$$H(jw) = \frac{1 - jw\tau}{1 + jw\tau}. \tag{1}$$

Here, τ is defined as the time constant. The group delay of the first-order APF can be derived using (1)

$$\tau_g = \frac{2\tau}{1 + (w\tau)^2}. \tag{2}$$

The group delay of the APF is maximized at the frequency of interest when

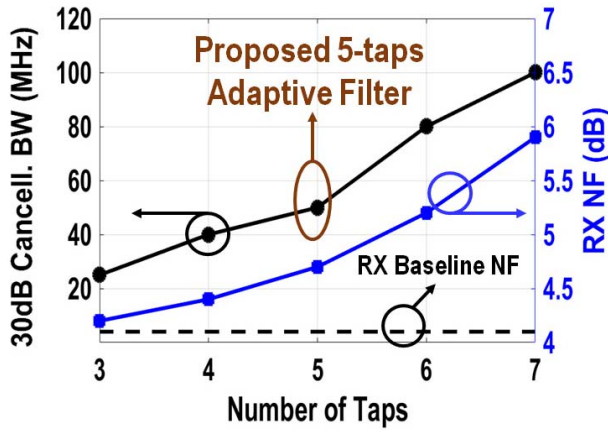$$\frac{\partial(\tau_g(\tau))}{\partial \tau} = 0. \tag{3}$$

Fig. 5. Design tradeoff among the number of taps, canceller noise and cancellation BW, and simulations performed in MATLAB Simulink and Cadence SpectreRF.

Fig. 6. Passive attenuator is introduced at the input of the RF canceller to improve linearity.

Solving (3) using (2) reveals that $\tau_g(jw)$ achieves a maximum when $\tau = (1/w)$

$$\tau_g(jw)_{\max} = \frac{1}{w} = \frac{1}{2\pi f}. \tag{4}$$

From (4), the maximum delay for each APF stage is limited by the operating frequency. In this design, the carrier frequency is 2 GHz and the maximum delay for each APF stage is 80 ps. If one applies the sampling theory to analyze the adaptive FIR filter, each tap samples the input signal at a different time and the output of each tap is summed using different gain values. An 80-ps tap-to-tap delay will be equivalent to a sampling frequency of 12.5 GHz, or an oversampling ratio of 3.14. To emulate the TX SI signal, the tap-to-tap delay must be sufficiently small to capture the fastest transient change in the SI signal. In addition, the total APF delay needs to be long enough to cover the SI signal delay spread [62]. The major contributions to SI in the RX are typically the shortest delay paths between the TX and the RX, which include direct coupling and antenna reflection paths [see Fig. 2(c)]. The delay spread between these two paths is approximately 250–350 ps. If the time delay in the RF canceller is designed to suppress the short-latency paths, 4–5 filter taps are sufficient. Additional taps help to suppress the TX leakage paths that arrive at the RX input at a later time, as compared to the two dominant TX-to-RX coupling signal paths. However, more taps will add more active devices and noise to the RX (see Fig. 5). Thus, in this design, it was found that five taps present an optimal based on the desire to achieve a 40-MHz cancellation BW, while minimizing the RX noise figure degradation.

An additional performance challenge associated with the design of both the RF and BB cancellers relates to the need for high linearity. The two feedforward cancellers on this chip take their inputs at the PA output, where the voltage may be large ($V_{\text{peak}} \sim 3$ V). This is in contrast to the canceller output, which is significantly lower in power/voltage amplitude (-15 dBm or 50 mV). Therefore, the linearity bottleneck of this feedforward canceller resides at the interface between the TX output and the canceller input. To accommodate a
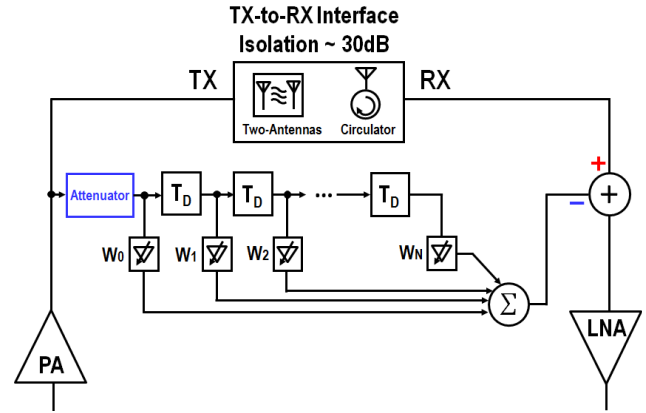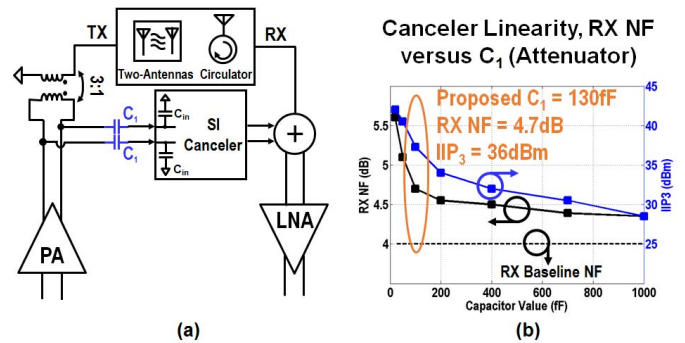

Fig. 7. RF canceller linearity versus attenuator capacitor C_1. (a) Conceptual diagram. (b) Simulation results of the capacitor value versus RX noise figure and canceller IIP$_3$.

high-output-power PA, the canceller must be designed to achieve as high a linearity as possible to minimize any intermodulation cross products generated along the feedforward canceller path which are directly injected into the RX, thus degrading the RX sensitivity.

To improve the cancellation paths' linearity performance, a passive attenuator (capacitive divider) was added at the PA—canceller interface (Fig. 6). The attenuator was implemented using a floating capacitor C_1, which is in series with the input capacitance of the RF canceller (C_{in}) [Fig. 7(a)]. However, any attenuation at the canceller input must be compensated for by providing more active voltage gain in the feedforward canceller, providing sufficient dynamic range at the canceller output, and ensuring gain matching between the TX leakage signal and this feedforward canceller output. As described in [63], additional voltage gain in the canceller signal path will have the effect of introducing/injecting more noise at the LNA/RX input. Thus, while introducing more attenuation in the cancellation path improves its linearity, this also has the effect of degrading the RX noise figure. A simulation illustrating the design tradeoff among the capacitor value, canceller IIP$_3$ and RX noise figure is shown in Fig. 7(b), where one observes that for a lower capacitor value C_1 (which provides a higher attenuation), the linearity improves, while the RX noise figure degrades. For this design, setting C_1
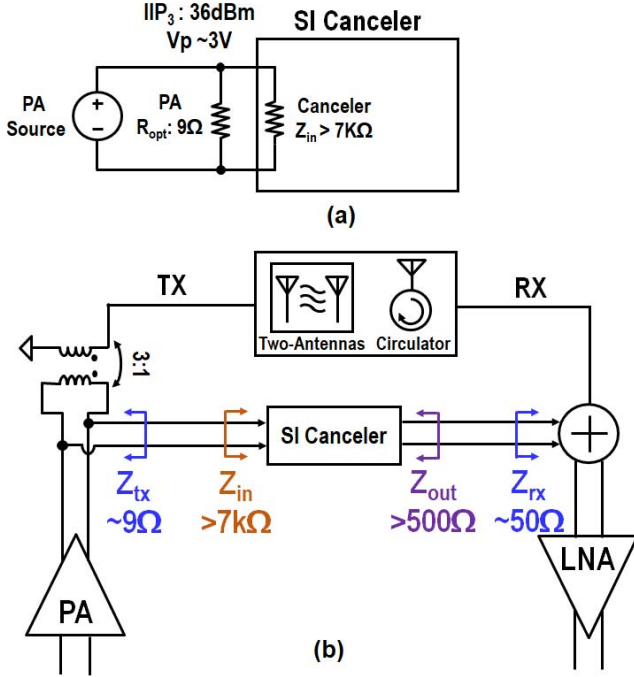
Fig. 8. RF canceller input–output impedance with the impedance seen by the canceller at the input–output. (a) Canceller input swing at 36 dBm IIP$_3$. (b) Canceller input–output impedance.

Fig. 9. Block-level diagram of the baseband cancellation path.

Fig. 10. Baseband canceller for attenuation of a TX carrier signal.

to match C_{in}, which is 130 fF, provides a good tradeoff among the attenuation (6 dB) at the canceller input, canceller linearity (+36 dBm), and the RX noise figure degradation (0.7 dB). The series capacitor C_1 has the additional benefit of increasing the input impedance looking into the canceller, which minimizes any loading on the PA output stage. For this design, the canceller real part input impedance is larger than 7 kΩ, which is significantly higher than the R_{opt} of the PA (see Fig. 8).

To further improve the linearity, the inputs of both cancellers are connected to the primary side of the PA output transformer that has a significantly lower impedance ($R_{opt} \sim 9$ Ω) as compared to the secondary side of the transformer that is connected to the 50-Ω antenna impedance. As such, the peak voltage on the primary side of the transformer (canceller input) is significantly lower ($V_{peak} \sim 3$ V), thus helping to further improve the canceller input-referred linearity. However, similar to the case of adding an attenuator (capacitor) at the canceller input to improve the linearity, tapping off the lowest impedance node at the PA output will reduce the effective canceller power gain, as described as

$$\text{Canceller power gain} = 10 \cdot \log_{10}\left(A_v^2 \cdot \frac{Z_{tx}}{Z_{rx}}\right). \quad (5)$$

Here, A_v is the canceller voltage gain, and Z_{tx} and Z_{rx} are the impedance from the perspective of the canceller input and output looking back into the TX and the RX, respectively. As an example, if Z_{tx} is 9 Ω and Z_{rx} is 50 Ω, this gives a 7.4-dB power attenuation due to the impedance transformation. To compensate for this power loss, the canceller signal path must provide an additional 7.4 dB of active voltage gain, which for this design was done with minimal impact on the RX NF.
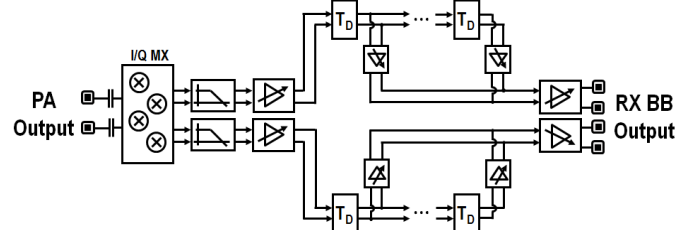
A high canceller output impedance is achieved using non-minimum length devices ($L = 65$ nm). The R_o looking into the canceller output is greater than 500 Ω, which is significantly higher than the LNA input impedance, thus having minimal impact on the LNA input matching network and S_{11}.

B. Second Baseband Canceller Signal Path

The design methodology for the BB canceller is similar to that of the RF canceller with a few significant differences that include: 1) using a larger time delay between the filter coefficients and 2) exploiting the use of highly correlated local oscillators to reduce the effects of reciprocal mixing of the TX leakage signal. The second BB cancellation path uses a downconversion mixer to translate the carrier frequency to BB. The BB feedforward canceller benefits from the cancellation signal being injected into the RX backend (analog BB). As such, there is significant RX gain prior to injection of the cancellation signal, thus relaxing the required noise performance of the BB canceller.

The BB cancellation path contains a 14-tap complex analog adaptive FIR filter with a downconversion quadrature mixer (Fig. 9). The BB canceller serves two functions: 1) it attenuates the TX SI carrier signal as well as the noise and non-linearities generated by the PA and TX and 2) it cancels the TX SI reciprocal mixing with the LO phase noise in the RX signal path. These concepts are described in the following.

The TX SI carrier signal travels in two paths. In one path, the TX SI signal passes through the circulator and down the RX chain, while in the other path, it travels through the BB canceller (see Fig. 10). Cancellation of the SI reciprocal
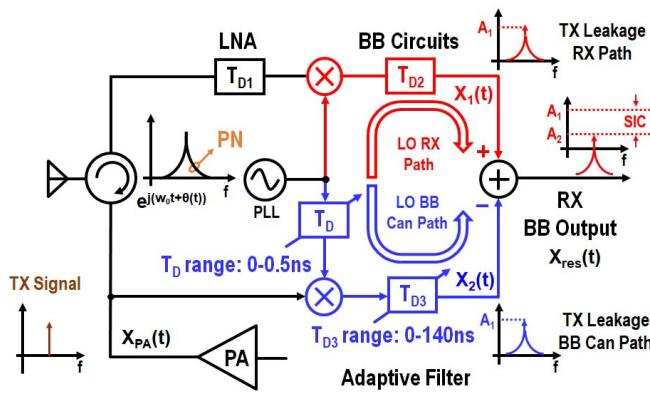
Fig. 11. Baseband canceller used to attenuate the TX leakage signal reciprocal mixing with LO phase noise in RX signal path.
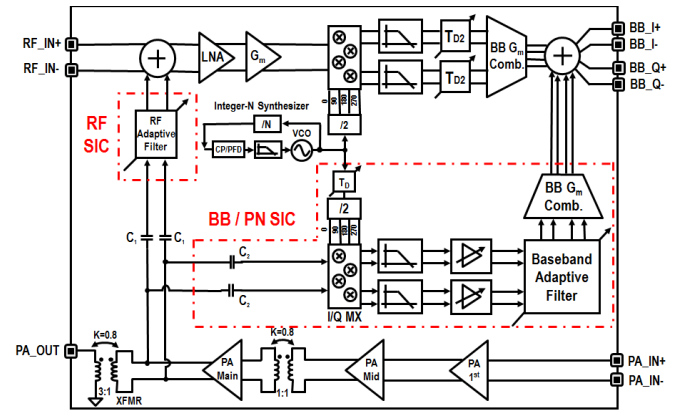

Fig. 12. System block diagram of components on the 40-nm CMOS FD system.
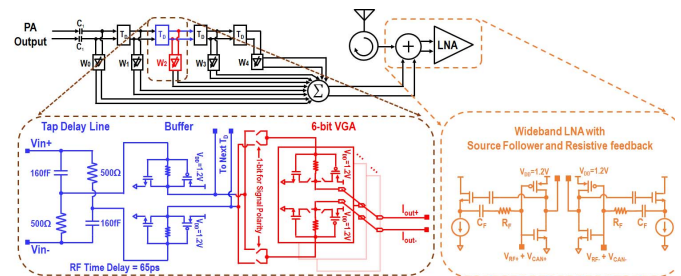

Fig. 13. Transistor-level implementation of the five-tap FIR-based RF canceller and the low-noise amplifier.

mixing in the RX and BB cancellation path mixers is achieved, if these two paths are matched in time. This design implements a combination of variable time delay blocks that includes T_D and T_{D3} to match the delay in the RX and the BB canceller signal paths (see Fig. 10).

The BB cancellation path attenuates the effects of reciprocal mixing between the TX SI signal and the LO phase noise in the RX signal path. This is shown conceptually, and for simplicity, as a single-tone continuous wave (CW) tone at the TX output (Fig. 11). Since the LO that supplies both the RX and BB cancellation path is derived from the same synthesizer, the phase noise of the LOs associated with the RX and BB canceller paths is highly correlated. Thus, if the time delays in the RX and BB cancellation paths are matched, the phase noise associated with the TX SI signal can be cancelled. A more mathematical analysis for this approach to cancel the TX SI reciprocal mixing products is given in the Appendix.

Intuitively, the adaptive FIR filter in the signal path of the BB canceller (T_{D3} in Fig. 11) matches any delay introduced by the BB circuitry in the RX signal path (T_{D2}). The additional delay in the LO path (T_D) is tunable to match the delay introduced from the circulator and front-end LNA (T_{D1}).

The above-mentioned analysis assumes a single short-delay leakage path. In the more realistic case with multiple leakage paths, including environmental reflections arriving with longer delays, this approach will be challenged to completely cancel the product of TX SI reciprocal mixing with the LO phase noise in the RX path. However, interference due to reflections with longer delays is received at a significantly lower power as compared to leakage paths with a short delay (e.g., direct coupling through the circulator). SI with lower power levels at the RX input results in reciprocal mixing products that are closer to the RX noise floor, having less impact on the carrier-to-interference ratio at the RX output. Thus, for this transceiver, a single delay unit (T_D) is designed to provide a compromise among the cancellation performance, power consumption, and silicon area.

Although the phase noise at both mixer ports due to the synthesizer and VCO is highly correlated, any phase noise introduced by the interconnect and circuitry (e.g., LO buffers and variable delay cell) along the two independent paths between the VCO and the mixers has no correlation. However,

the phase noise associated with a VCO and synthesizer often dominates any phase noise contributed by open-loop buffers and interconnect, particularly close to the carrier. This relates to the fact that noise inside a synthesizer is correlated, integrating from one period to the next, while broadband thermal noise introduced by buffers, interconnect, or delay cells outside the synthesizer loop lack an integrative process. In this design, the measured phase noise floor of the synthesizer is −155 dBc/Hz; however, the simulated noise produced by the variable delay cell is −167 dBc/Hz, resulting in minimal impact on the RX NF. Post-cancellation, a potential major source of phase noise and reciprocal mixing, could come from the noise generated by the delay cells and buffers, in the two independent LO paths.

IV. CIRCUIT IMPLEMENTATION

A block diagram of the dual injection-path FD front-end transceiver is shown in Fig. 12, which illustrates all the components integrated on the chip. This chip includes an RX chain from the LNA input to an analog BB output, an integer-N PLL, a noise cancelling PA, and two integrated feedforward cancellers. All the signal paths are designed differentially to minimize the TX-to-RX isolation, while improving the even-order distortion performance.

A. RF Canceller and RX LNA

The RF canceller is made up of a five-tap analog FIR filter (Fig. 13). Each of the tap delay lines is implemented using a
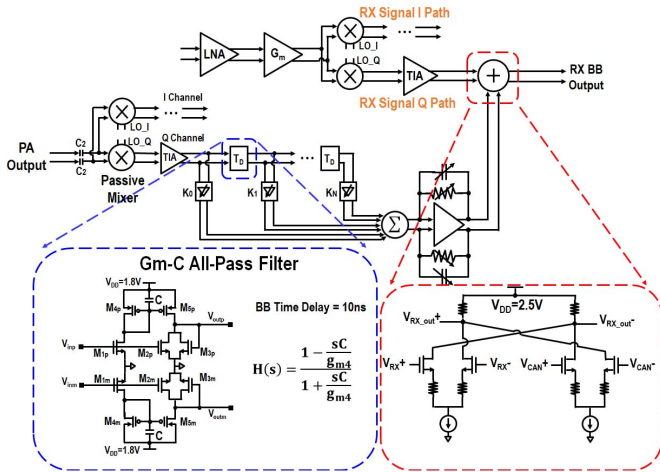
Fig. 14. Transistor-level implementation of the 14-tap FIR-based BB canceller with the output summing stage.

Fig. 15. Transistor-level implementation of the three-stage class AB power amplifier.

passive *RC–CR* first-order APF. This APF functions as a true-time delay cell with a nominal delay of 65 ps. The variable gain amplifier (VGA) was implemented as a 6-bit inverter-based amplifier with one additional bit that determines the signal polarity. An additional bit in the VGA will provide 6 dB more dynamic range and better cancellation; however, this also has the effect of reducing the output impedance of the canceller by half, loading the impedance at the LNA input, which increases the RX input insertion loss. The RF canceller was designed with a gain range from −60 to −25 dB to emulate the magnitude response of the leakage channel. The maximum gain of the RF canceller is set to 5 dB higher than the expected magnitude of the maximum leakage signal to provide some design margin. A unity-gain buffer stage was added between each tap delay to buffer each of the APFs. The output of each filter/gain stage is summed in the current domain, with the ac signal coming from the RX input (antenna) (Fig. 13). The RX LNA uses resistive feedback to achieve a broadband 50-Ω match (Fig. 13) [64], [65]. A CMOS implementation of the LNA increases the effective G_m by nearly a factor of 2, which aids in reducing the LNA noise figure. A source follower is added to avoid the direct feedforward path from the LNA input to the output, which effectively increases the LNA output impedance, gain, and improves the NF [66].

B. Baseband Canceller

The BB cancellation path is implemented with two 14-tap analog FIR filters and a passive downconversion mixer (see Fig. 14). Each of the tap-delay elements have a desired delay significantly higher (10 ns) than the RF analog FIR. If the same *RC–CR* circuit was used to realize the delays as was done at RF, the on-chip implementation would be prohibitively large (at least 10× as compared to the RF equivalent. Thus, the BB FIR tap-delay elements were implemented using a compact G_m-*C*-based APF described in [67]–[69]. The output of each tap is summed in the current domain, then translated to the voltage domain using a transimpedance amplifier. The BB
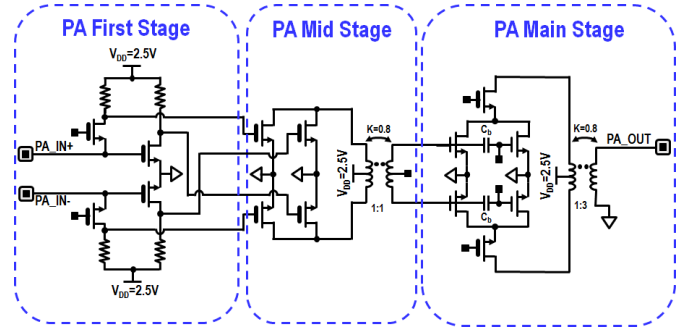
canceller signal is combined with the desired RX signal using a resistor-degenerated common-source amplifier (Fig. 14). The BB canceller simulated flicker noise corner is 500 kHz, which minimizes the impact on the RX NF.

C. Power Amplifier

This FD radio integrates a three-stage class-AB PA (Fig. 15), with the input coming from an off-chip signal generator. A common-source, common-gate noise-cancelling topology, which is similar to what has been often used in low-noise amplifier designs, is implemented as the first stage of the PA, to reduce the PA thermal noise floor [70], [71]. It is worth noting that the PA noise cancelling topology is only beneficial when the rest of TX is off chip, and the PA demands 50Ω input impedance; a fully integrated TX would likely not benefit from this topology. To improve the linearity of the PA, a G_m-linearization technique was realized similar to [72] and [73]. The input devices of the PA output stage are divided into two separate devices. The larger device is biased closer to the class-A region, while the auxiliary device is biased closer to the class-B region to linearize the effective G_m over a wide range of the input voltages. The PA operates off a 2.5 V supply.

D. Remaining Integrated Transceiver Components

The RX chain contains a low-noise amplifier, G_m stage, and passive mixers, followed by a transimpedance amplifier. The mixer is driven by a four-phase 25% duty cycle LO, which was generated from a divide-by-two circuit [74]. The tunable time delay cell in the LO path, used for the BB canceller (see Fig. 10), implements a current starving topology, which is similar to [60] and [75] and has a simulated resolution (LSB) of 0.5 ps with a tuning range of more than one period of the carrier. This is equivalent to a 0.36° resolution with a 0.5-ns tuning range at 2 GHz. To improve the phase noise performance of the integer-N synthesizer, an impulse sensitivity function (ISF) manipulation technique similar to [76] is used to lower the phase noise performance of the voltage-controlled oscillator.

The chip was fabricated in a 40-nm six-metal-layer Taiwan semiconductor manufacturing company (TSMC) CMOS process and occupies an area of 1.75 mm × 2 mm that includes the bond pads (Fig. 16). The chip was wire bonded directly to the test-board using chip-on-board packaging.
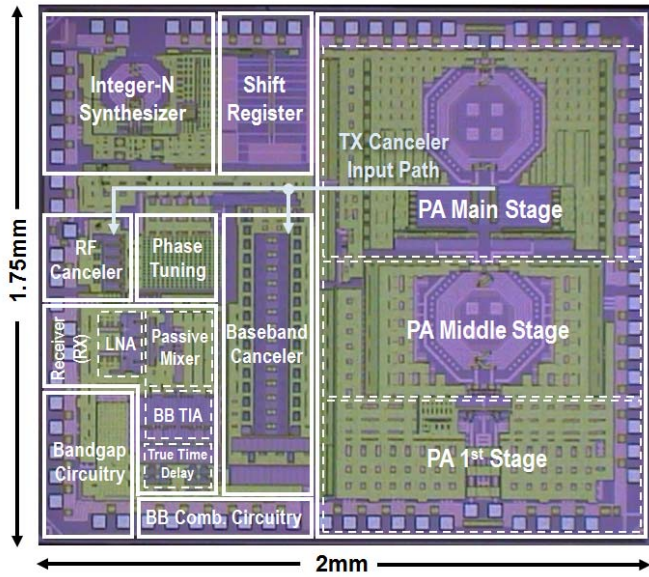
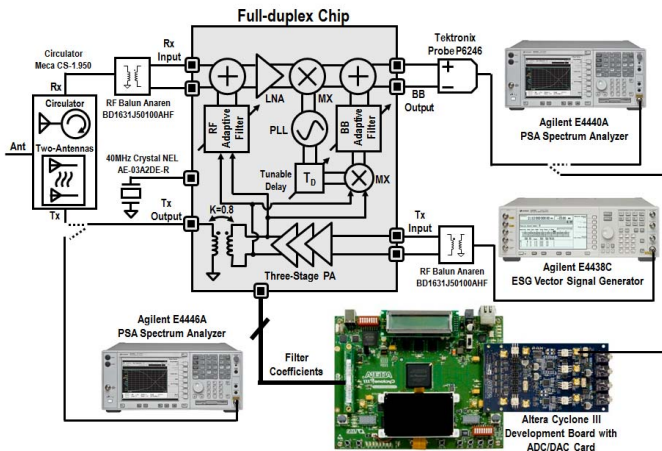Fig. 16. FD die photograph. Device implemented in a six-metal-layer TSMC 40 nm.

Fig. 17. Measurement setup for the FD chip.

V. MEASUREMENT RESULTS

To test the functionality of the proposed FD chip, the standard RF measurements were performed to characterize the gain, noise, linearity, and depth/BW of SI cancellation with the cancellers enabled and disabled; the measurement setup is shown in Fig. 17. During testing, there was an option of using two configurations for the RF front-end interface, mainly either two antennas or a discrete circulator (MECA Electronics: CS-1.950), both of which could provide an isolation as high as 30 dB. An air interface that is realized with two antennas typically has a group delay larger than 2 ns, and thus, there will be a non-negligible time delay mismatch between the RF canceller (range 250–350ps) and the leakage channel (>2 ns), which will lead to less cancellation in the RF domain. The cable routing from the chip TX output to the circulator, to the RX input, were kept as short as possible, to minimize the delay mismatch between the leakage and the cancellation paths. Two surface-mount singled-ended-to-

differential baluns (Anaren: BD1631J50100AHF) were used to present a balanced input to both the RX and the TX input. The RX BB quadrature output signals were connected to two low-noise high-input-impedance (>200 kΩ, <1 pF) active differential probes (Tektronix: P6246), to buffer the chip BB outputs, while providing 50-Ω matching to the next stage, which could be either a spectrum analyzer (Agilent E4440A) or a discrete 14-bit 140-MSPS analog-to-digital converter (Analog Devices: AD9254). The reference clock of the integer-N synthesizer uses a low-noise crystal oscillator (NEL Frequency Controls: AE-03A2DE-R/40.000 MHz). Section V begins with the circulator serving as the leakage channel, where the antenna port is connected to a 50-Ω termination. Another set of measurements using two antennas is provided with a discussion, at the end of this section.

While performing closed-loop TX SI cancellation testing, a CW or modulated signal was applied to the PA input from a vector signal generator (Agilent E4438C). The analog-to-digital converter (ADC) sampled the RX BB output signal, which was a downconverted version of the TX SI signal, averaged the RX BB signal over ten cycles, and then sent it back to an field programmable gate array (FPGA) board (Altera Cyclone III EP3C120 Development Board) for post-processing. The FPGA board emulates what would otherwise be a digital BB to implement a closed-loop calibration for the analog FIR filters in both the feedforward cancellation paths and the tunable delay element used to suppress the reciprocal mixing of the TX SI. A blind source adaptation algorithm was used to adapt the coefficients of all the filter taps, where the algorithm begins the adaption process on the five-tap RF canceller first. After the RF canceller filter taps converge, the adaptation algorithm then calibrates the BB complex IQ cancellation filters.

All measurements were taken using five different test boards and chips.

A. Standard RF Measurements

The RX operates from 1.7 to 2.2 GHz with a measured maximum gain of 36 dB, 3-dB BW of 12 MHz, and a 4-dB in-band noise figure. The measured in-band IIP$_3$ and $P_{-1\,\text{dB}}$ of the RX is -5 and -15 dBm, respectively. The entire RX consumes 22 mW from a 1.2-/2.5-V power supply.

The PA has a measured output $P_{-1\,\text{dB}}/P_{\text{sat}}$ of 25.1/26.5 dBm and a maximum PAE of 32% [see Fig. 18(a)]. The PA error vector magnitude (EVM) was measured to be 5.1% EVM when a 40 Mb/s 16QAM signal with $+20$-dBm output power was used [see Fig. 18(b)].

The integer-N synthesizer has a measured locking range from 3.4 to 4.4 GHz, while consuming 10.4 mW from a 1.2-V supply with a phase noise of -116 dBc/Hz @ 1 MHz offset at a center frequency of 4 GHz. The reference spur of the synthesizer is -55 dBc.

The RF/BB canceller is supplied by 1.2/1.8 V and has a measured $P_{-1\,\text{dB}}$ and IIP$_3$ of 27/26.5 and 36/34.5 dBm, respectively. These linearity numbers were reported using a two-tone test by enabling only the last taps of RF/BB canceller with a maximum gain, while disabling the remaining taps. The
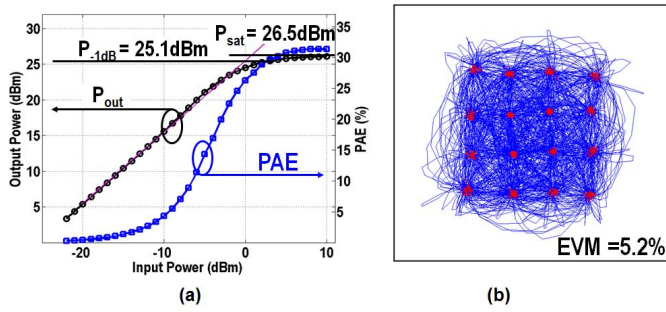
Fig. 18. Measured PA performance. (a) PA output power and efficiency with a single tone input at 1.96 GHz. (b) PA EVM testing with an input of 40 Mbp/s 16-QAM signal and an average PA output power of 20 dBm at a center frequency of 1.96 GHz.

Fig. 19. Measurement results of TX SI suppression versus bandwidth.

two-tone signals were injected at the output of TX (canceller input), and the intermodulation products were measured at the RX input. During the measurement, the PA was turned on to provide a low impedance ($R_{opt} \sim 9\ \Omega$) at the canceller input. The transformer insertion loss was de-embedded from the measurement based on the simulation results (IL ~ 1.5 dB). The purpose of this measurement was to characterize the worst case linearity of the canceller, since the last taps see the most gain and are the dominant contributor of non-linearities in the active canceller chain, thus leading to a worst case linearity performance. When the same measurements were repeated using only the first tap of the RF canceller, the results of $P_{-1\,dB}$ and IIP$_3$ are to be improved to 32 and 42.5 dBm, respectively.

B. SI Cancellation Measurements With Circulator

To characterize the functionality of the feedforward cancellers, both CW and modulated signals were applied to the TX input, while both the cancellation depth and the BW were measured by observing the residual TX SI at the RX BB output. The RX 3-dB BW is 12 MHz, which is insufficiently high to allow a flat response in the BB. This was a design oversight on the chip, as the BB I/Q BW should be higher than 20 MHz for a 40-MHz signal. However, the measurement was taken with the canceller both on and off using the narrower BW (12 MHz). Thus, the reported cancellation number is independent of the RX BB band edge.

Applying a CW signal to the PA input, the cancellation BW was measured in two steps. First, the cancellation was maximized at a center frequency by adapting the coefficients of both cancelling filters. Then, while holding the feedforward FIR filter settings, a series of CW signals with different frequencies were swept across the band. This measurement reveals that a minimum 50-dB cancellation was achieved within the 42-MHz cancellation BW (see Fig. 19). The TX SI cancellation measurement was then repeated using a modulated signal. A 40 MHz 16QAM signal with an average output power of 15 dBm was applied to the TX input, while the RX output spectrum was measured with both the cancellation network enabled and disabled. From these measurements, more than 50 dB of SI cancellation was achieved, which is consistent with the test results when using a CW input (see Fig. 20).
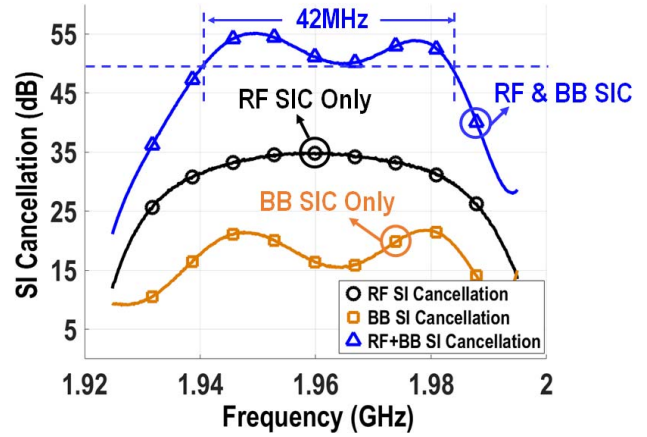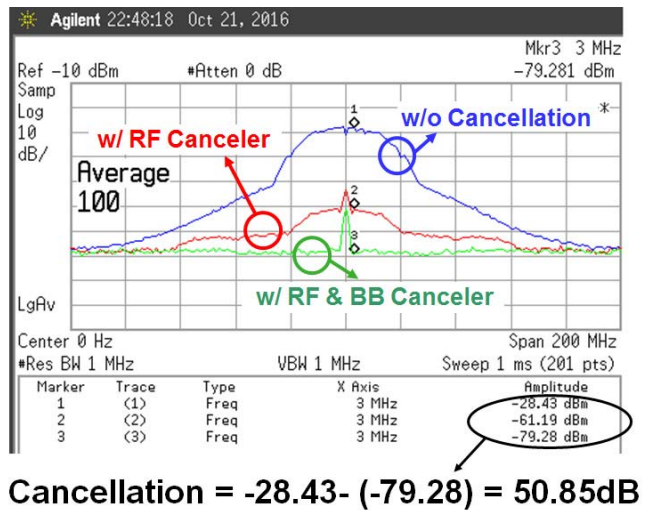

Fig. 20. Measured TX suppression using a modulated 40 Mb/s 16QAM signal. RX baseband output spectrum with cancellers enabled and disabled.

A two-tone test was performed to characterize the canceller linearity performance. This measurement was taken by applying two in-band tones with equal amplitude to the canceller input while the RX BB output was measured, in the case of the cancellers enabled and disabled (see Fig. 21). When the cancellers are enabled, the amplitude of third-order intermodulation products generated by the cancellers is equivalent to the fundamental tone at a 17-dBm PA output power. If the PA is operated above 17 dBm, the residual SI signal after cancellation will be limited by the canceller third-order non-linearity. The canceller linearity could be further improved by adding more attenuation at the canceller input, which will be traded off with the RX noise figure (see Fig. 7). The canceller effective IIP$_3$ with respect to RX/antenna input, while testing the SI cancellation testing is +17 dBm.

The required IM3 in the link budget depends on the modulation scheme. In a multi-carrier system, if the PA operates at 10 dBm or higher, the absolute IM3 generated by the canceller is still above the RX noise floor. Thus, in order to operate this PA with full power (25 dBm) in the FD mode, the canceller
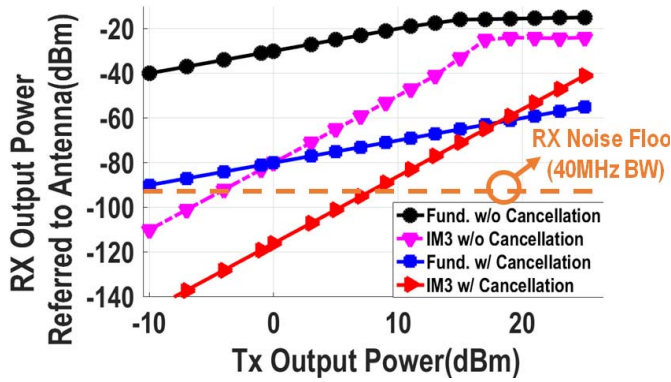
Fig. 21. Two-tone linearity testing for the cancellers, measured with two tones and IM3 components of the TX SI signal all referred to the antenna with the cancellers enabled and disabled.
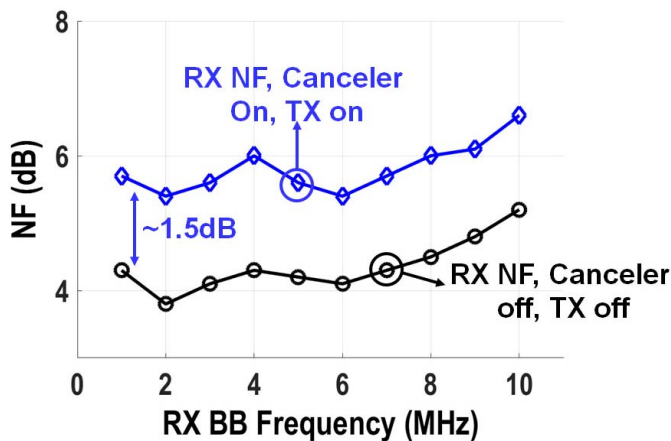

Fig. 22. Measured RX noise figure with +15-dBm blocker with the canceller enabled and disabled relative to the baseband frequency.

IIP$_3$ needs to be as high as 50 dBm to guarantee that the canceller-generated IM3 is lower than the RX noise floor. In contrast, the IIP$_3$ required of the canceller would be relaxed if the radio was operating with a modulated signal using a single-carrier.

The RX NF degradation due to the introduction of the feedforward cancellers is another key performance metric to adequately characterize the FD transceiver. The RX NF measurements in FD mode were performed using a desired single-tone RX signal, which were set 100 kHz away from the TX carrier signal, while monitoring the carrier-to-interference (C/I) ratio at the RX BB output; the results are shown in Fig. 22. The black curve is the measured RX baseline NF with the TX turned off and the canceller disabled. Next, the TX is enabled with the PA output set to 15 dBm. After enabling both cancelling filters, the RX NF degradation was determined to be 1.55 dB.

To characterize the cancellation of TX SI signal reciprocal mixing with the LO phase noise in the RX signal path, a CW signal is applied to the PA input while the RX BB output spectrum is measured, with the BB canceller and the additional time delay block T_D, enabled and disabled [see Fig. 23(a)]. The measurement result shows a 10-dB suppression [see Fig. 23(b)].

(a)

(b)
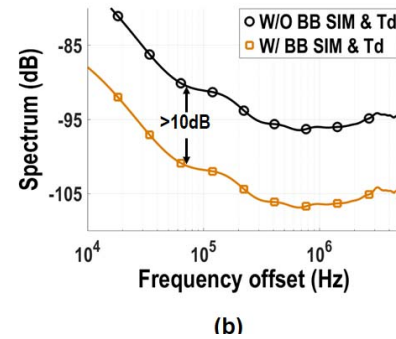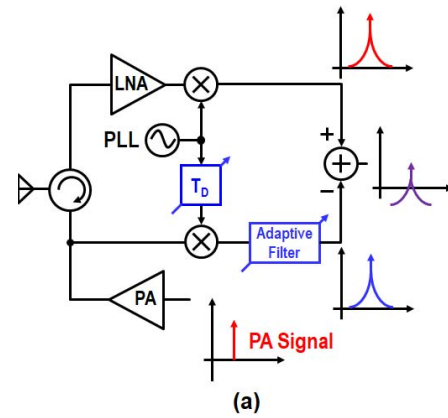
Fig. 23. Measured suppression of the TX SI signal reciprocal mixing with RX LO phase noise in the RX signal path. (a) Measurement setup. (b) Measurement results at the RX baseband output with cancellation enabled and disabled.
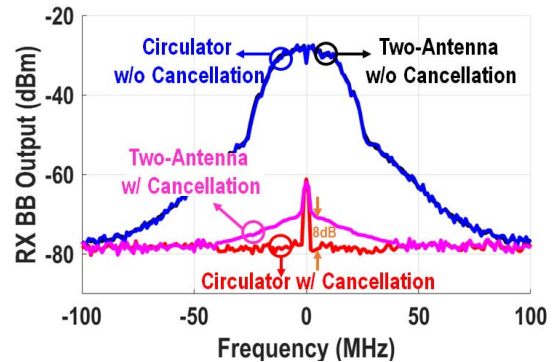
Fig. 24. Measured TX suppression using a modulated 40 Mb/s 16QAM signal with a circulator and two-antenna as leakage channel. RX baseband output spectrum with cancellers enabled and disabled.

C. SI Cancellation Measurements With Two-Antennas

The SI cancellation measurement was repeated using two antennas to serve as the air interface. The leakage channel from two antennas can produce a group delay up to ~2 ns. The SI cancellation results using a modulated signal (40 Mb/s 16-QAM) are shown in Fig. 24. The larger group delay introduced from the two antennas creates a non-negligible time delay mismatch between the leakage path and the RF canceller. This degrades the cancellation by 8 dB (worst case) as compared to using an air interface that includes a circulator and a single antenna.

The total chip power consumption is 49 mW, excluding the PA (see Fig. 25). A comparison and performance summary is shown in Table I.

TABLE I
COMPARISON AND PERFORMANCE SUMMARY

		J. Zhou ISSCC' 2015	D.-J van den Broek ISSCC' 2015	D. Yang JSSC' 2015	J. Zhou ISSCC' 2016	This Work
Architecture		Frequency Domain Equalization	Mixer-First RX+ VM-downmixer	Mixer First+ Duplexing LNA	Integrated Circulator+ BB SIC	Adaptive Filter + NC PA+ LO Sideband Suppression
Technology/VDD		65nm /?	65nm/1.2V	65nm/1.2V, 2.5V	65nm/1.3V, 2.2V	40nm /1.2, 1.8V, 2.5V
RX Frequency (GHz)		0.8-1.4	0.15-3.5	0.1-1.5	0.6-0.8	1.7-2.2
TX-to-RX Interface Isolation (dB)		30-50	N/A	N/A	N/A	30-35
Integrated Power Amplifier		No	Yes	Yes	No	Yes
Integrated PLL		No	No	No	No	Yes
TX Maximum Suppression (dB)		N/A	27	33	N/A	55ⁱ
Cancellation BW	Cancellation (dB)	20	27	33	42ᶠ	50ⁱ
	BW (MHz)	15 / 25ᵃ	16.25ᶜ	0.3	12ᶠ	42ⁱ
RX NF degradation due to leakage cancellation (dB)		0.9-1.2/1.1-1.5ᵃ	4-6	N/Aᵉ	5.9ᵍ	1.05 (RF)+0.5(BB)
Canceler Power Consumption (mW)		44-91ᵇ	N/A	N/A	30	3.5 (RF) +8 (BB)
RX IB IIP₃ (dBm)		-20 @ 27dB gain	+9/19 at 24dB gain	-38.7 @ 53dB gain	-33 at 42dB gain	-5 at 30dB gain
RX In-Band SC-FD P-₁dB with Cancellation (dBm)		>-8	>1.5	-17.3	N/A	+3
Effective IIP₃ with respect to RX/ANT Input (dBm)		+2 at 27dB gain	21.5 at 24dB gain	N/A	+1 at 42dB gain	+17 at 30dB gain
RF Canceler Area (µm²)		N/A	N/A	N/A	N/A	203 × 124
Canceler IIP₃ (dBm)		N/A	N/A	N/A	N/A	36 (RF) / 34.5 (BB)
Canceler P-₁dB (dBm)		N/A	N/A	N/A	N/A	27 (RF) / 26.5 (BB)
RX LO Sideband Suppression (dB)		N/A	N/A	N/A	N/A	10
RX Gain		27-42	24	33-53	42	20-36
RX Power Consumption (mW)		63-69	23-56ᵈ	43-56	70ʰ	22
Maximum TX Output Power (dBm)		N/A	>10	N/A	N/A	25
TX PAE (%) @Maximum Power		N/A	N/A	N/A	N/A	32
TX EVM (%)		N/A	N/A	N/A	N/A	5.1
PLL Phase Noise @1MHz (dBc/Hz)		N/A	N/A	N/A	N/A	-116
Active Area (mm²)		4.8	2	1.5	1.4	3.5

ᵃ Measurement with an antenna pair. 15MHz BW, 0.9-1.2dB NF deg. is with one filter. 25MHz, 1.1-1.5dB NF deg. is with two filters. ᵇ Power including 0-47mW Gm cells and 44mW LO for one filter.
ᶜ Half-duplex/Full-duplex mode show NF of 6.3/ 10.3-12.3dB. ᵈ Power including LO tree. ᵉ RX DSB NF is 5-8dB in Full-Duplex mode.
ᶠ 42dB cancellation 12MHz BW measured including integrated circulator, not including 43dB digital cancellation from Matlab.
ᵍ The TDD RX NF is 5dB, NF increases to 8.4dB including the circulator and goes to 10.9dB including the baseband canceller. ʰ Power Including 60mW signal path and 10mW LO path at 0.7GHz.
ⁱ The measured maximum 55dB cancellation and 50dB cancellation over 40MHz BW doesn't include the 30-35 dB isolation from the discrete circulator or two-antennas.
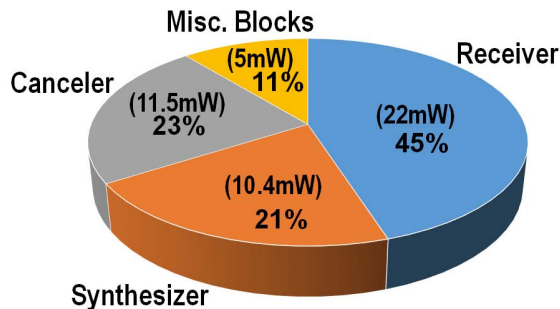
Fig. 25. FD transceiver power breakdown. This excludes the PA that dissipates up to 1 W.

cancellation BW (>42 MHz) with the highest SI cancellation (>50 dB), compared to the state of the art. The proposed front end includes two feedforward cancellers, which are both implemented as analog FIR filters to provide an inverse response of the leakage channel. The first coarse canceller is attached at the RX input to relax the linearity requirements of LNA and the subsequent RX blocks, while the second finer canceller injects its output into the RX BB.

Future wireless applications could potentially have both the FD and FDD modes. When network traffic is low, FDD would likely be more optimal from a power consumption perspective. With more wireless traffic and a demand for higher data rates, the device would have the option of moving to a FD mode of communication.

VI. CONCLUSION

This paper demonstrates a dual-injection path FD wireless transceiver system that achieves a combination of the broadest

APPENDIX

$X_{PA}(t)$ is the PA output signal, and $X_1(t)$ and $X_2(t)$ are the leakage and canceller signal before the summing stage

(Fig. 11). The LO signal with phase noise is modeled with $e^{j(w_0 t + \theta(t))}$. In this analysis, we assume that there is no amplitude mismatch between the leakage and the canceller signal. From Fig. 11, $X_1(t)$ and $X_2(t)$ could be derived as

$$X_1(t) = X_{\mathrm{PA}}(t - T_{D1} - T_{D2}) \times e^{j(w_0(t - T_{D2}) + \theta(t - T_{D2}))} \quad (6)$$

$$X_2(t) = X_{\mathrm{PA}}(t - T_{D3}) \times e^{j(w_0(t - T_D - T_{D3}) + \theta(t - T_D - T_{D3}))}. \quad (7)$$

In order to achieve TX SI cancellation, $X_1(t)$ and $X_2(t)$ have to be equal, therefore combining (6) and (7) gives

$$T_{D3} = T_{D1} + T_{D2} \quad (8)$$

$$T_D = -T_{D1}. \quad (9)$$

In this design, T_D is implemented with a digital variable time delay block that has a tuning range of one carrier cycle; therefore, T_D could also be modeled as a $360°$ phase rotator. Moreover, the negative sign in (9) could be realized with a simple $180°$ phase shift.

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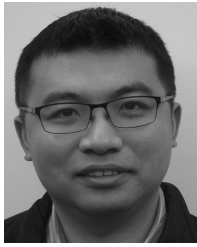
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