A Precision Wideband Quadrature Generation Technique With Feedback Control for Millimeter-Wave Communication Systems

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***Abstract*— An integrated two-stage polyphase filter (PPF) with feedback control for quadrature local oscillator generation at millimeter-wave frequencies is described. To minimize the in-phase (I) and quadrature (Q) mismatch, the second stage of the PPF utilizes triode-region nMOS transistors to implement variable resistors where the resistance is precisely controlled by modulating the shared gate-to-source bias voltage at the gate of nMOS devices. The gate bias voltage of the triode-region devices is set by a feedback loop which changes with variations in process, voltage, and temperature. A prototype quadrature signal generator, employing this PPF design, is integrated in a 28-nm LP CMOS process. A worst case measured phase/amplitude imbalance of 2°/0.32 dB (typical–typical corner dies) and 2.2°/0.55 dB (slow–slow corner dies) is reported over 7-GHz bandwidth for a fixed control current (I_{Ctrl}). By retuning I_{Ctrl} at every 7 GHz, this IQ generator would maintain the measured quadrature accuracy from 55 to 70 GHz. The core area occupied by the IQ generator circuitry is 20 μm × 40 μm and the device consumes less than 192 μW, of which 120/72 μW comes from the feedback control-loop/opamp, respectively. The proposed PPF method has a simulated input impedance of 150 Ω in-parallel with 18 fF.**

***Index Terms*— CMOS integrated circuits, feedback circuits, millimeter-wave (mm-wave) integrated circuits, quadrature generation.**

I. Introduction

OVER the past two decades, there has been a drastic increase in the bandwidth (BW) and data rates for smart phones and notebook computers. At present, existing commercial standards in the RF bands (1–6 GHz), such as wideband code division multiple access [1], [2], local thermal equilibrium [3], [4], and Wi-Fi [5], [6] provide as much as 160-MHz BW with data rates as high as 1000 Mb/s per user.

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The demand for more accessible BW and higher data rate is predicted to grow as the next-generation communication systems; that is, 5G is expected to support 1000 times higher data per area, and 10–100 times higher data rates per user (10–100 Gb/s) with as much as 10× extension in battery life compared to existing solutions [7], [8]. The RF spectrum, in the 1–6-GHz band, has become increasingly crowded with incremental improvements in spectral efficiency through higher order signal modulation schemes, e.g., 1024 QAM. Utilizing a higher order modulation method alone is insufficient to achieve a factor of 10–100× data rate improvement as demanded by 5G communication systems. Multi-input multi-output (MIMO) systems can achieve higher spectral efficiencies via spatial multiplexing at the expense of system complexity, power consumption, and cost [6], [9]. Likewise, new hardware which enables full-duplex transmission by applying self-interference cancellation methods [10]–[20] would allow a single radio to simultaneously transmit and receive using the same frequency band (full-duplex communication). However, under ideal conditions, a full-duplex transceiver improves the throughput by no more than a factor of two, again significantly less than the 10× desired by the future fifth generation wireless systems.

While the low-frequency gigahertz bands are saturated, communication in the millimeter-wave (mm-wave) bands presents an attractive solution for evolving 5G standards [21], [22]. The vast spectrum available at mm-wave frequencies allows wireless service providers to significantly expand the channel BWs far beyond 20 MHz, e.g., 2.16-GHz BW for 802.11ad standard [23]. Successful CMOS implementations of mm-wave transceivers which achieve data rates between 1 and 10 Gb/s have been reported [24]–[27]. Recent developments in mm-wave transceivers have focused on enabling channel bonding [24], MIMO [28], and in-band full-duplex techniques [29], in an attempt to push data rates beyond 10 Gb/s.

At lower frequencies (<10 GHz), direct-conversion (zero-IF) transceiver architectures are commonly used in both RX and TX due to the resulting simplicity of the RX/TX signals paths and compatibility with integration. However, utilizing a direct-conversion architecture to realize a mm-wave transceiver requires I–Q signals that are highly phase accurate (90°), with a minimal amplitude mismatch. Fig. 1 shows

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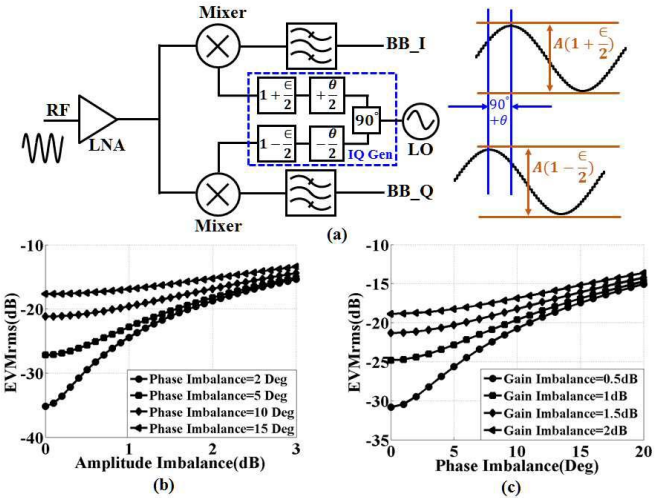

Fig. 1. Impact of quadrature imbalance. (a) Quadrature imbalance in a typical transceiver. (b) EVM variations with gain imbalance. (c) EVM variations with phase imbalance.

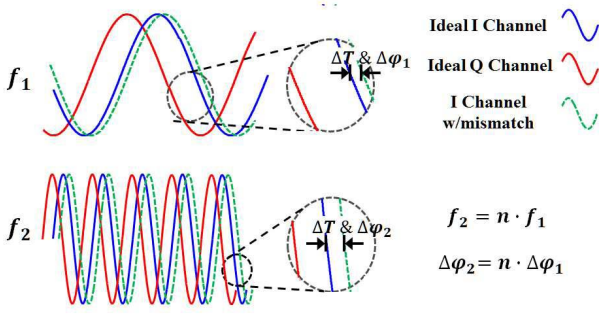

Fig. 2. Illustration of phase imbalance at low and high frequencies due to a mismatch-induced timing error.

a simple model that illustrates the challenge of generating a highly quadrature accurate signals in the mm-wave band, particularly for DC transceivers where the error-vector-magnitude (EVM) performance is typically dominated by the local oscillator (LO) phase and amplitude mismatch. For a direct-conversion receiver, the IQ imbalance increases the receiver's EVM and hence its bit error rate (BER) [30] This mismatch could be mitigated by using digital baseband calibration [31]; however, this requires a loop-back method from the TX to RX, which complicates the radio transceiver design, especially at mm-wave frequencies [31]. Furthermore, in many future applications, especially for low-cost and low-power systems, the modems must be kept very simple and a complicated digital calibration circuitry will have too high of a power penalty.

The realization of a highly balanced IQ generator, without requiring digital calibration, is one of the most challenging aspects of an mm-wave transceiver design. This is due to an increased sensitivity of quadrature phase and gain accuracy, for a given mismatch, as the frequency rises. Fig. 2 illustrates this concept of phase imbalance as a function of frequency, for a given mismatch timing delay error. A constant time delay mismatch ΔT is dependent on the mismatch in device geometry and is relatively independent of frequency. For example, an LO IQ mismatch of 1°, at 6 GHz, from a delay mismatch ΔT, would increase to 10° at 60 GHz (see Fig. 2) [32].

This paper seeks to realize a generic wideband mm-wave quadrature generation technique which is readily implemented for mm-wave applications, including 60-GHz transceivers (e.g., 802.11ad). Moreover, this technique is equally applicable to any low-frequency gigahertz-band transceiver design requiring high-accuracy quadrature signals. This paper is organized as follows. Section II overviews existing, state-of-the-art quadrature generation techniques. A detailed description of a proposed two-stage polyphase filter (PPF)-based quadrature generator (QG) with feedback control is given in Section III. Section IV presents design considerations for the proposed PPF. Circuit implementation details of the PPF and integrated phase measurement circuitry implemented in a 28-nm CMOS process are given in Section V, while measurement results of the QG prototype are provided in Section VI. Last, a few concluding comments are given in Section VII.

II. State-of-the-Art: Quadrature Generation

Ideally, to minimize the impact on EVM and BER, a QG should provide I/Q signals with equal amplitude and a 90° phase difference, over the frequency band of interest. An ideal integrated quadrature signal generator would have the following characteristics.

1) Perform precision quadrature balance while utilizing minimal silicon area.
2) Result in minimal insertion loss.
3) Have minimal power consumption.
4) Present a large input impedance to relax the loading effects on the previous stage (i.e., voltage-controlled oscillator (VCO) or driver amplifier).
5) Minimize the sensitivity to process, voltage, and temperature (PVT) variations.

Three commonly employed methods to generate I/Q LO signals include: 1) quadrature VCOs (QVCOs); 2) divide-by-two circuits with a VCO running at twice the LO frequency; and 3) a PPF. Other methods, which are more often used for mm-wave band applications include differential branch-line directional couplers [33], distributed microstrip shunt stubs [34], and quadrature all-pass filters [35], [36].

QVCOs use two cross-coupled oscillators that inherently produce a 90° phase difference between the outputs. Tradeoffs exist with QVCOs between the coupling strength, I/Q phase accuracy, tuning range, and the phase noise (PN) performance. Divide-by-two circuits generate I/Q signals from a VCO running at twice the desired LO frequency; however, the VCO must operate at double the carrier frequency (e.g., 120 GHz for a 60-GHz transceiver), which degrades the PN performance, reduces the frequency tuning range, and increases the power consumption due to the low quality factor of the passive components at a higher operating frequency [37]. Transmission line-based methods mentioned in [33]–[35] often occupy substantial silicon area to realize the mm-wave IQ generation circuitry, in addition to being relatively narrowband.

A PPF is able to generate precision quadrature LO signals with fractional BWs (FBW = BW/center frequency) exceeding 30% by cascading more than two stages [38]–[40]. However, the insertion loss of each PPF stage limits the number of

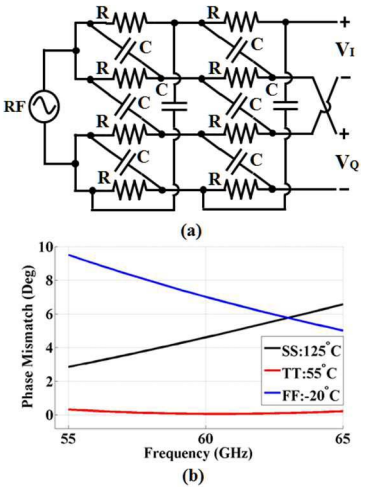

Fig. 3. Phase mismatch in two-stage PPFs plotted for several process and temperature corners. (a) Schematic of a two-stage PPF. (b) Simulation results of phase mismatch.

stages, hence restricting its practical use to narrowband systems. Furthermore, the IQ balance of a PPF is dependent on the *RC* product. Given that each *R* and *C* may vary by as much as 30% over process and temperature, which will cause the *RC* product to vary by as much as 70%. The simulated IQ phase mismatch of a typical two-stage PPF simulated over different process corners and temperature from −20 °C to 125 °C, spanning a frequency range from 55 to 65 GHz, is shown in Fig. 3. Both stages are sized to operate at 60 GHz using the typical–typical corner (TT) at 55 °C. The phase mismatch is shown to be less than 0.5° over a BW of 7 GHz. However, the phase mismatch will increase if the *RC* product varies as a function of the PVT corners. The worst case corners in this particular process happen in the slow–slow corner (SS) at high temperature (125 °C) or in the fast–fast corner (FF) at low temperature (−20 °C). In these corners, the resistor and capacitor values move in the same direction, either increase together (SS, 125 °C), or decrease together (FF, −20 °C). This leads to a PVT phase mismatch from TT-to-FF and TT-to-SS of up to 10°, due to variation in the resistor and capacitor values.

The remainder of this paper describes a generic, yet novel, I/Q generation technique which attempts to address all the aforementioned ideal characteristics using a calibrated *N*-stage PPF. This is followed by an expanded description of the prototype mm-wave quadrature generation technique first described in [41]–[43].

III. Proposed PPF-Based Quadrature Generator

This quadrature generation technique is derived from the traditional *N*-stage PPF implementation. As shown in Fig. 3, the phase imbalance of a PPF is sensitive to PVT variations, thus the importance to introduce calibration circuitry which accurately controls the component values used by the PPF. The analysis of phase imbalance is carried out on an *N*-stage PPF in [44]. This paper focuses on a two-stage PPF for a couple of reasons. First, the device which was implemented and measured is a two-stage PPF. Second, the analysis leads to a more intuitive understanding of why tuning a single

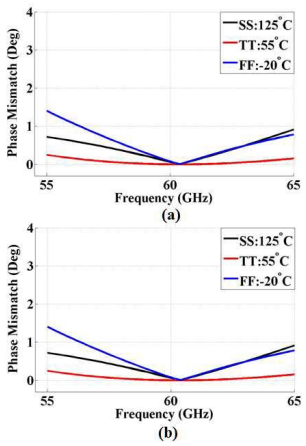

Fig. 4. Phase imbalance of two-stage PPFs with only one stage *R*, *C* value accurately controlled. (a) First stage with PVT variations, second stage without PVT variations. (b) First stage without PVT variations, second stage with PVT variations.

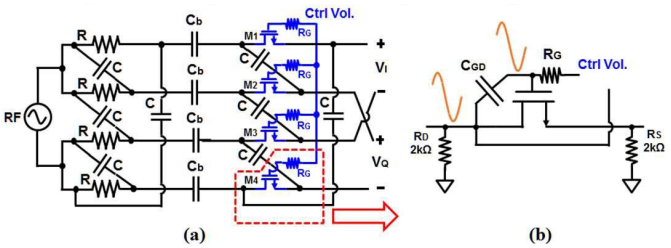

Fig. 5. Proposed two-stage PPF with feedback control. (a) Schematic of proposed circuit. (b) Description of auxiliary bias resistors added for the triode-region transistors.

stage in a multistage PPF is sufficient to obtain highly accurate quadrature signals, as opposed to tuning each stage. In short, the calibration concepts valid for a two-stage PPF are extendable to an *N*-stage PPF implementation. Fig. 4 shows the simulated phase imbalance of a two-stage PPF where one stage is precisely controlled. Compared to Fig. 3, the simulated phase mismatch using the two extreme process and temperature corners (SS, 125 °C and FF, −20 °C), shown in Fig. 4, is less than 1.5° over a frequency range from 55 to 65 GHz. This mismatch is sufficient to meet the EVM required by the 60-GHz 802.11ad standard [24], [30]. In addition, tuning the *RC* product of just the second stage in a two-stage PPF, while leaving the first stage untuned, produces identical phase accuracy results, as compared to tuning just the first stage, while leaving the second stage untuned (Fig. 4). The phase difference between the output *I* and *Q* signals is given in the following equation:

$$\angle\frac{V_Q}{V_I}(\omega) = 2\cdot\tan^{-1}\frac{\omega(R_1C_1+R_2C_2)}{(1+R_1C_1R_2C_2\omega^2)}. \tag{1}$$

Here, R_1C_1/R_2C_2 is the first-/second-stage component values of a PPF. Assuming, $x = \omega R_1C_1$, $y = \omega R_2C_2$, (1) simplifies to

$$\angle\frac{V_Q}{V_I}(\omega) = 2\cdot\tan^{-1}\frac{x+y}{1+xy}. \tag{2}$$

From (2), the output phase balance has an equal dependence on the *RC* product of the first and second stages of a PPF. Thus, having precise control over the *RC* product of any one stage

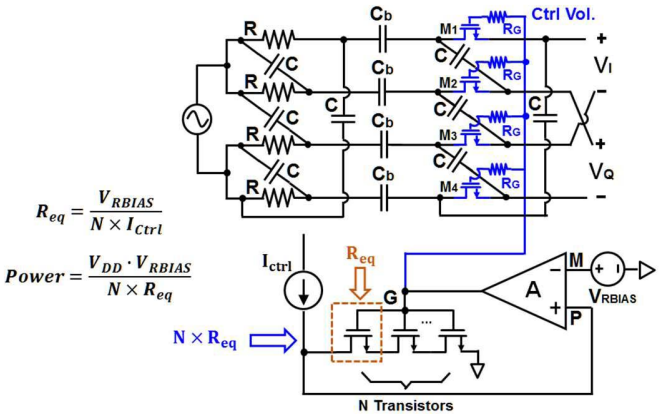

Fig. 6. Feedback circuitry for the proposed two-stage PPF.

of an N-stage PPF will produce the same quadrature phase error.

In the proposed IQ generation circuit (Fig. 5), the second stage is precisely controlled to generate accurate IQ signals taking into account the loading effects on the previous stage, either an oscillator or buffer output. The tuning is achieved by replacing the resistors in one stage, with triode-region transistors. This allows precise control of the channel resistance. Calibrating the capacitor values of a PPF will serve a similar function. However, at mm-wave frequencies, both switched-capacitor banks and varactors show a poor quality factor (<10) and hence the PPF contributes a large insertion loss [45]. DC blocking capacitors C_b [Fig. 5(a)] and additional bias resistors R_S and R_D [Fig. 5(b)] are added to set the dc operating point of the source and drain of the triode-region device, ensuring the transistor remains in triode region. In addition, a 2-kΩ poly-resistor R_G is placed in series with gate of each nMOS transistor, to ensure the device maintains a relatively constant source-to-gate voltage, and thus a constant channel resistance. Without R_G, the large voltage swing of the LO would appear across the gate and source/drain of the nMOS transistor, thus modulating its channel resistance. A feedback network drives the gate voltage of the triode-region transistors to set the desired channel resistance independent of variation in process, temperature, and supply voltage (Fig. 6). The feedback network includes an operational amplifier, N replica transistors in the triode region that are identical to the nMOS transistors of the PPF, a fixed (bandgap) bias voltage V_{RBIAS}, and a constant control current I_{Ctrl}. With the feedback loop closed, the equivalent channel resistance of each nMOS transistor R_{eq} in the PPF is given by V_{RBIAS} and I_{Ctrl} as

$$R_{\mathrm{eq}} = \frac{V_{\mathrm{RBIAS}}}{N \times I_{\mathrm{Ctrl}}}. \tag{3}$$

The channel resistance R_{eq} is insensitive to the PVT variations, since all variables in (3) V_{RBIAS}, I_{Ctrl}, and N are, to the first order, insensitive to PVT variations.

A detailed circuit diagram of the proposed structure is shown in Fig. 6, where there are N times as many replica transistors placed in series as compared to the device used in the PPF. Given the high frequency associated with mm-wave circuits, the nominal resistance value required in the PPF is as low as (∼200 Ω), leading to large values of I_{Ctrl}. Thus, to reduce the power, the resistance in the replica is made N times larger to reduce the value of I_{Ctrl}, by a factor N. For example, in our implementation of a two-stage PPF, $N = 3$ which reduces I_{Ctrl} and the power, by a factor of 3. The power of this PPF architecture is described by

$$\text{Power Consumption} = V_{\mathrm{RBIAS}} \times I_{\mathrm{Ctrl}} = \frac{V_{\mathrm{DD}} \times V_{\mathrm{RBIAS}}}{N \times R_{\mathrm{eq}}}. \tag{4}$$

It is noteworthy that only one replica bias control loop is necessary in an N-stage PPF; thus, the power necessary to tune the N-stage PPF will be the same for any value of N. However, compared to a traditional N-stage PPF, which typically uses polysilicon resistors, a triode-region transistor has more parasitic capacitance (C_{GS}, C_{GD}, C_{DS}, and etc), that leads to a higher insertion loss. Thus, a tradeoff exists between the number of stages with triode-region devices used for calibration, quadrature imbalance over the BW of interest, and the insertion loss. This replica technique could be extended to each of the four triode-region transistors used in a single stage, by creating four dedicated replica bias feedback loops, to better calibrate any mismatch between each of the resistors in a single stage of the PPF. However, this would be done at the expense of slightly higher power consumption and occupying more silicon area to accommodate four opamps, in addition to requiring a longer calibration time.

IV. PPF-Based Quadrature Generation Design Issues

Several practical design issues arise in the realization of the proposed PPF-based QG. These include designing for a high input impedance, low insertion loss, minimizing the impact of parasitic capacitance, the design of the feedback-loop opamp, low noise, and a layout strategy to minimize parasitics in the PPF.

A. Input Impedance

To minimize the effects of loading on the component driving the QG (either a VCO or a driver amplifier), the PPF should ideally have as large an input impedance as possible. For a given LO frequency, the PPF RC product is a known constant based on the frequency of operation. The input impedance is dominated by the R and C of the first stage [38]. This implies that picking a large resistor size leads to a high PPF input impedance.

However, several practical considerations limit the size of the resistors. First, all the resistors are in the LO signal path; thus, their noise contribution will rise with an increase in the value of R. Assuming the same values of R and C are used in each stage, of a multistage PPF, the voltage noise spectral density at the PPF output will be dominated by the resistors in the later stages, approximately 4kTR [38]. Therefore, an upper bound to the resistor values in the PPF will be determined by an acceptable level of the broadband LO PN floor (large offsets from carrier). The PN produced by an mm-wave VCO and phase-locked loop (PLL) is on average worse than the equivalent frequency generation in the lower RF bands. As such, the resistor thermal noise produced by the PPF will

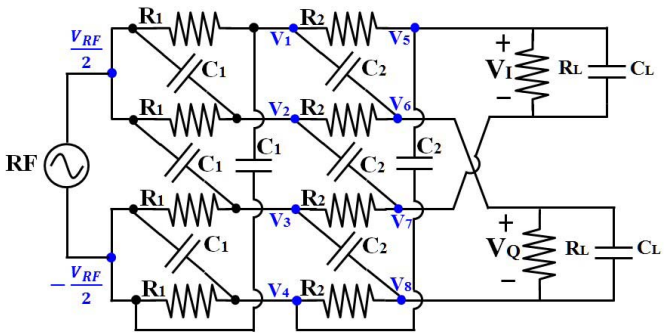

Fig. 7. Optimal sizing of two-stage PPF considering the loading effect.

be negligible as compared to the PN produced by mm-wave PLL. However, if a similar PPF technique is applied to lower frequency RF applications, then the resistor noise produced at large offset frequencies could be appreciable as compared to the synthesizer PN. See Section IV-E for more thorough discussion on noise performance. Second, all the resistors integrated in silicon have a cutoff frequency, due to the parasitic capacitance to substrate, which will introduce a phase imbalance between I and Q. This implies that for a given sheet resistivity, larger size resistors create more parasitic capacitance, thus increasing an unwanted phase shift [38], [46]. Last, the resistor size is further limited by parasitic considerations of the capacitor. Naturally, as the resistor is made larger, for a given frequency, the capacitor size must be lowered. However, if the capacitor size is too small, both the parasitic capacitance and the effects of capacitor mismatch will begin to impact circuit performance [47]. Considering all the aforementioned effects, the proposed PPF nominally uses 14.8-fF capacitors and 179-Ω resistors. Extracted layout simulation results show the input impedance to be 150 Ω in parallel with 18 fF at the LO center frequency of 60 GHz.

B. Insertion Loss

Both the PPF insertion loss and input impedance influence the required number of buffer stages and ultimately the power consumption of the overall solution, including the VCO, PPF, and buffers. Thus, the insertion loss of the PPF must be minimized. Fig. 7 shows a two-stage PPF where the load capacitance and resistance are modeled. The insertion loss can be described by

$$\mathrm{IL} = \frac{\sqrt{|V_I|^2 + |V_Q|^2}}{|V_{\mathrm{RF}}|} = \frac{\sqrt{|V_5 - V_7|^2 + |V_6 - V_8|^2}}{|V_{\mathrm{RF}}|}. \quad (5)$$

Exploiting the symmetry of the circuit, (5) simplifies to

$$\mathrm{IL} = \frac{\sqrt{|2V_5|^2 + |2V_6|^2}}{|V_{\mathrm{RF}}|} = \frac{2\sqrt{|V_5|^2 + |V_6|^2}}{|V_{\mathrm{RF}}|}. \quad (6)$$

Applying Kirchoff's current and voltage laws to the circuit in Fig. 7 yields (7), as shown at the bottom of this page, where $Z_L = R_L \| \, 1/sC_L$.

Assuming the RC product for each stage is constant, the insertion loss reduces to (8), as shown at the bottom of this page, where $m = R_2/R_1 = C_1/C_2$. Near the center frequency, where $\omega \approx (1/R_1C_1)$, (8) simplifies to

$$\mathrm{IL}(m) \approx \left| \frac{2\sqrt{2} \cdot \left(\frac{1}{R_1^2} + \omega^2 C_1^2 - \frac{2 \cdot j\omega C_1}{R_1} \right)}{\frac{4(m+1)\left(\frac{1}{R_1} + j\omega C_1\right)}{Z_L} + 2\left(1 + \frac{1}{m}\right) \cdot \left(\frac{1}{R_1} + j\omega C_1\right)^2} \right|. \quad (9)$$

The insertion loss is minimized when

$$\frac{\partial \mathrm{IL}(m)}{\partial m} = 0. \quad (10)$$

Solving (9) using (10) gives

$$m_{\mathrm{opt}} = \frac{1}{\sqrt{2}} \cdot \sqrt[4]{\frac{\frac{1}{R_1^2} + \omega^2 C_1^2}{\frac{1}{R_L^2} + \omega^2 C_L^2}}. \quad (11)$$

The procedure to size the components used by the implemented PPF is summarized as follows.

1) Pick the first-stage R_1 and C_1 values for the desired LO frequency, input impedance, and PN floor.
2) Simulate the extracted load impedance as seen by the PPF output.
3) Pick the optimal m from (11) and size the second stage of the PPF according to $R_2 = m_{\mathrm{opt}} \times R_1$ and $C_2 = C_1/m_{\mathrm{opt}}$.

Fig. 8 shows simulation results of normalized insertion loss as a function of frequency and m, where m is a scaling factor. The first and second stages have R and C values of 179 Ω and 14.8 fF and 179 × m Ω and 14.8/m fF, respectively. From the simulation, the optimal insertion loss happens when m is close to 0.75, which matches with (11) and results in a 0.3-dB insertion loss reduction as compared to $m = 1$. Next, the impact of parasitic capacitance associated with the triode-region device is explored in the context of phase accuracy and insertion loss.

$$\mathrm{IL} = \left| \frac{\sqrt{2} \cdot Z_L \left(\frac{1}{R_1 R_2} - \frac{sC_1}{R_2} - \frac{sC_2}{R_1} - s^2 C_2 C_1 \right)}{2s\,(C_2 + C_1) + 2\left(\frac{1}{R_1} + \frac{1}{R_2}\right) + Z_L\left(\left(\frac{1}{R_2} + sC_2\right) \cdot \left[s\,(C_1 + C_2) + \frac{1}{R_2} + \frac{1}{R_1} \right] - s^2 C_2^2 - \frac{1}{R_2^2}\right)} \right| \quad (7)$$

$$\mathrm{IL} = \left| \frac{2\sqrt{2} \cdot \left(\frac{1}{R_1^2} + \omega^2 C_1^2 - \frac{2 \cdot \mathrm{j}\omega C_1}{R_1} \right)}{\frac{4(m+1)\left(\frac{1}{R_1} + j\omega C_1\right)}{Z_L} + 2\left(1 + \frac{1}{m}\right) \cdot \left(\frac{1}{R_1} + \mathrm{j}\omega C_1\right)^2 + \frac{2}{m}\left(\omega^2 C_1^2 - \frac{1}{R_1^2}\right)} \right| \quad (8)$$

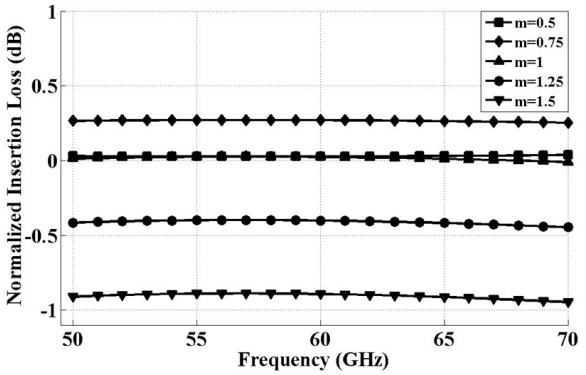

Fig. 8. Simulation results of normalized insertion loss as a function of frequency with different values of m.

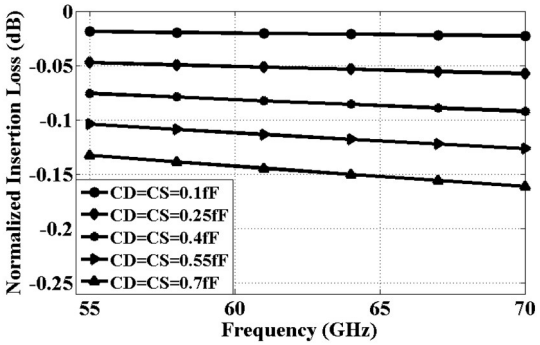

Fig. 10. Simulation results of normalized insertion loss of two-stage PPF as a function of frequency with different values of C_D and C_S.

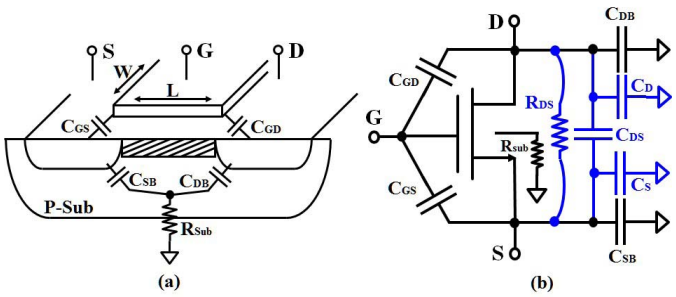

Fig. 9. Triode-region transistor model with parasitic capacitance. (a) Cross section of a MOS transistor. (b) Simplified schematic model of a MOS transistor.

C. Parasitic Capacitance

The proposed technique uses triode-region transistors to realize the second-stage resistors, which will introduce unwanted parasitic capacitance and further affect the amplitude/phase mismatch and insertion loss.

A cross section of a triode-region transistor model [48] is shown in Fig. 9(a). This model includes capacitance from the gate-to-source ($C_{\rm GS}$), drain-to-gate ($C_{\rm GD}$), source/drain-to-bulk ($C_{\rm SB}/C_{\rm DB}$), and the substrate resistance $R_{\rm sub}$. This model simplifies all the drain and source capacitance to ground as one lumped capacitance at the drain and source, named C_D and C_S, respectively [Fig. 9(b)]. A nonnegligible source-to-drain capacitance must also be taken into consideration for several reasons. First, a 2-kΩ poly-resistor is placed in series with the gate of each triode-region transistor which ensures the gate impedance is high even at mm-wave frequencies (see Fig. 5). $C_{\rm GS}$ and $C_{\rm GD}$ are in series with the gate resistor, thus forming a series C–R voltage divider from the perspective of the drain-to-gate and source-to-gate. Second, in a deep submicrometer technology, the source and drain are routed with metals interconnect, which are close to each other. The metal-to-metal sidewall capacitance between the source and drain fingers introduces a nonnegligible parasitic capacitance, represented as $C_{\rm DS}$, which is included in a lumped-element model [Fig. 9(b)]. Although this parasitic capacitance is small, usually less than 0.5 fF for a minimum length and width transistor, it will introduce an amplitude mismatch between the I and Q signals, as well as increasing the insertion loss. The impact of C_D, C_S, and $C_{\rm DS}$ on the insertion loss and amplitude/phase mismatch will now be explored.

Any additional C_D and C_S will have minimal impact on the amplitude/phase mismatch at the PPF output, as this is equivalent to equal loading among all PPF output ports. However, C_D and C_S will function as a current divider at the output of each PPF stage, which has the effect of increasing the insertion loss. Generally, if $C_S \ll C_1+2C_L$ and $C_D \ll C_1 + C_2$, where C_1 and C_2 are the first and second stage capacitance of the PPF, respectively, while C_L is the load capacitance, then the insertion loss is minimal. Fig. 10 shows the simulation results of normalized insertion loss of a two-stage PPF as a function of frequency with different values of C_D and C_S. This simulation was performed using ideal resistors and capacitors in both stages of the PPF, modeled with additional parasitic capacitance. From the simulation, if parasitic capacitance C_S and C_D are less than 0.7 fF, the insertion loss will be less than 0.155 dB. In the actual design, the triode-region transistors are sized at a minimum length (2.4 μm/28 nm) to reduce parasitic capacitance C_S and C_D. C_S and C_D are further reduced by placing the devices inside a deep N-well which creates less than 0.5 fF of parasitic capacitance.

The indirect coupling from the drain-to-source produces an effective capacitance $C_{\rm DS}$, which introduces an amplitude mismatch by providing a coupling path from the output of first stage to the second stage. The simulation results of amplitude/phase mismatch and normalized insertion loss of a two-stage PPF as a function of frequency with different values of $C_{\rm DS}$ are shown in Fig. 11. From simulation, C_S, C_D, and $C_{\rm DS}$ will have negligible impact on amplitude/phase mismatch and insertion loss, if the capacitance is less than 0.5 fF.

As mentioned earlier, minimum size triode-region transistors are desired to reduce unwanted parasitic capacitance. Thus, the performance of this PPF calibration technique will improve with the future technology scaling, as the unwanted parasitic capacitance scales down.

D. Opamp Design

The PPF tuning circuit includes a feedback loop to modulate the channel resistance of the replica devices shown in Fig. 6.

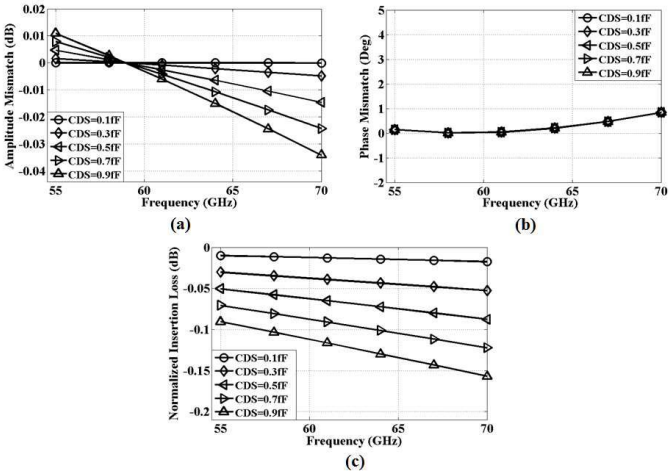

Fig. 11. Simulation results of amplitude/phase mismatch, normalized insertion loss of two-stage PPF as a function of frequency with different values of C_{DS}. (a) Amplitude mismatch. (b) Phase mismatch. (c) Normalized insertion loss.

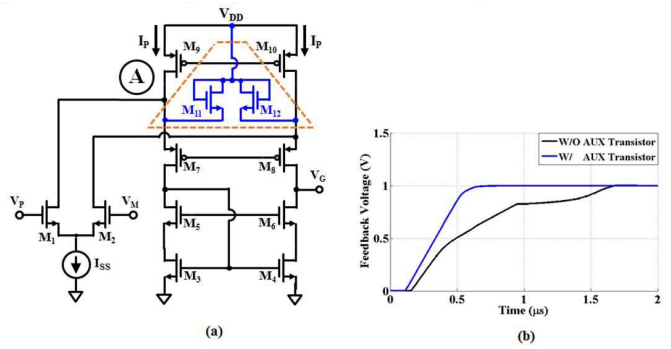

Fig. 12. Schematic of the opamp and the settling time of the proposed feedback loop. (a) Opamp schematic with a folded-cascode topology. (b) Proposed feedback loop settling time.

The loop transfer function is made up of the opamp input-to-output response and gain from the V_G (opamp output) to V_P (opamp positive input). The small-signal gain from V_G to V_P is analyzed below.

Assuming all the stacked transistors are operated in triode region and sized equally, V_P can be expressed as

$$V_P = \sum_{i=1}^{N} V_{\mathrm{DS}_i} = \frac{I_{\mathrm{Ctrl}}}{\mu_n C_{\mathrm{ox}} \frac{W}{L}} \sum_{i=1}^{N} \frac{1}{V_{\mathrm{GS}_i} - V_{\mathrm{th}}} \approx \frac{I_{\mathrm{Ctrl}}}{\mu_n C_{\mathrm{ox}} \frac{W}{L}}. \tag{12}$$

Using (12), the small-signal gain between V_G and V_P can be expressed as

$$\frac{\partial V_P}{\partial V_G} = \frac{\mathrm{NI}_{\mathrm{Ctrl}}}{\mu_n C_{\mathrm{ox}} \frac{W}{L}} \times \frac{-1}{\left(V_G - V_{\mathrm{th}} - \frac{(N-1)\cdot V_{\mathrm{RBIAS}}}{2N}\right)^2}. \tag{13}$$

Assuming each cascode device has the same V_{ds}, this gives

$$I_{\mathrm{Ctrl}} = \mu_n C_{\mathrm{ox}} \frac{W}{L} (V_G - V_{\mathrm{th}}) \frac{V_{\mathrm{RBIAS}}}{N}. \tag{14}$$

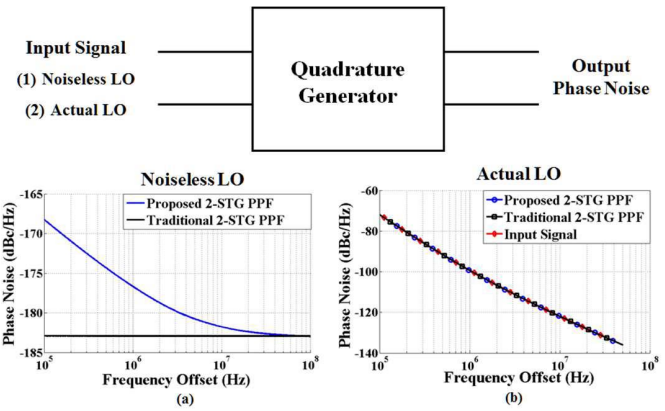

Fig. 13. PN simulation of the proposed QG versus traditional two-stage PPF with an ideal 60-GHz LO and realistic 60-GHz LO input. (a) Simulation taken with a noiseless LO. (b) Simulation taken with an actual LO.

Combining (13) and (14) yields

$$A_{\mathrm{PG}} = \left|\frac{\partial V_P}{\partial V_G}\right| = \frac{V_{\mathrm{RBIAS}}}{V_G - V_{\mathrm{th}}}. \tag{15}$$

Equation (15) further reveals the loop stability is independent of the number of cascoded transistors. In this design, V_{RBIAS} is nominally a fixed voltage of 100 mV. However, V_G varies from 0.7 to 1.05 V, to achieve a desired resistor tuning range from 120 to 520 Ω. Lower V_{RBIAS} could help to reduce the power consumption of the PPF [see (4)], but the calibration would become more sensitive to the opamp input offset voltage. Also, the PPF power consumption is lower bounded by the opamp.

A folded-cascode opamp with an open loop gain of 80 dB is designed for the feedback loop [Fig. 12(a)]. From simulation, when the feedback loop is enabled, it takes 1.5 μs to settle the control voltage [Fig. 12(b)]. The settling behavior of the feedback loop deviates from the traditional characteristics of an OTA in feedback. To minimize the power consumption, the current I_P in the pMOS active load is smaller than the tail current I_{SS}. Thus, while V_G (opamp output) is charging up the load capacitance, M_7 turns OFF and the voltage at node A falls to a level that pushes M_1 and the tail current source (shown as ideal) into the triode region [Fig. 12(a)]. This slows down the opamp and creates unusual "kinks" in the settling behavior. The slew rate of the opamp can be improved by clamping node A to V_{DD}, using transistors M_{11} and M_{12} [49] [Fig. 12(b)]. This produces a settling response shown in blue curve [Fig. 12(b)].

E. Noise

Compared to the traditional two-stage PPF, with passive polysilicon resistors R and metal–oxide–metal (MOM) capacitor C, the proposed structure replaces polysilicon resistors with active devices, which in turn may degrade the LO PN.

Fig. 13(a) shows the simulated PN plots at the output of a traditional and the proposed PPFs using a noiseless LO as the input. As expected, the PN of the traditional PPF exhibits a flat spectrum due to the thermal noise contribution

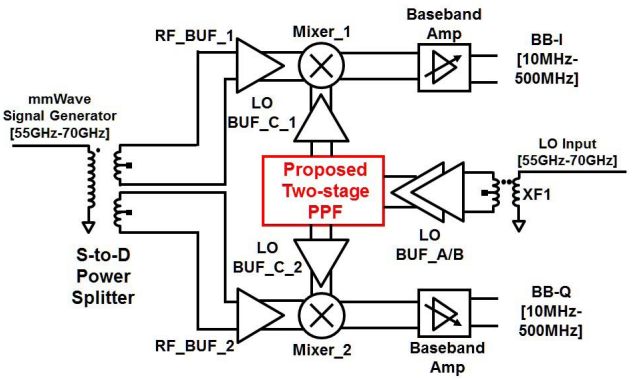

Fig. 14. Block diagram of the proposed system for IQ balance measurements.

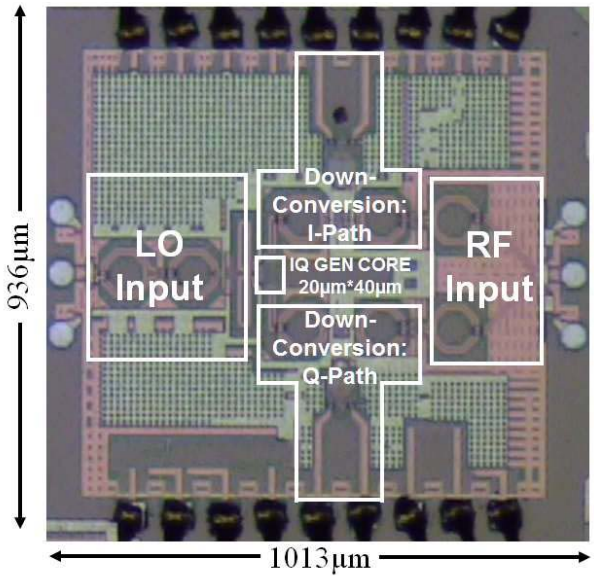

Fig. 15. Seven-layer metal GlobalFoundries 28-nm quadrature generation chip micrograph.

of the polysilicon resistors. The proposed PPF structure shows higher PN contribution, which is mainly attributed to the active devices in the PPF and feedback circuitry. However, a real PLL has a PN profile which is significantly higher than the PN contributed by the resistors in the PPF. Fig. 13(b) shows a PN simulation result with an actual LO signal as the input of a PPF. This simulation models the PN of the VCO and synthesizer by modeling the LO input signal to the PPF with a PN profile with data from a state-of-the-art 60-GHz frequency synthesizer, given in [50]. The PN simulations are performed with a 1-V peak-to-peak swing applied to the PPF input. As such, the noise from opamp, control current/voltage, and replica transistors have been taken into account with these simulation results. The simulation shows almost the same input–output PN performance with both a traditional and the proposed PPF structures [see Fig. 13(b)]. Thus, the noise added by the PPF circuitry is negligible.

F. Layout Techniques

An L-compensated approach, which is identical to [51], is employed to reduce the layout-related asymmetry and further improve the quadrature balance.

V. Measurement Circuit Implementation

Two methods are commonly used to measure and characterize the quadrature imbalance. The first approach measures the IQ phase imbalance directly at the carrier frequency (mm-wave band) using high-frequency probes. However, the measurement accuracy becomes limited by the phase mismatch introduced by the probes, the cables, the differential balance of the input signal, and the finite short-open-load-termination calibration accuracy at mm-wave frequencies. The second approach attempts to perform the IQ accuracy at a lower frequency by first down-converting the LOs where an accurate IQ imbalance measurement can be done. However, the down-converter design mandates the use of large device sizes in the amplifiers, mixers, and buffers to minimize any mismatch introduced by the test circuitry. The method used in this device down-converts the LO before sending the signals off-chip where accurate measurements are easier to obtain.

Two down-conversion mixers with linear buffers were used to measure the quadrature phase and gain accuracy (see Fig. 14). A single-to-differential (STD) power splitter is used to generate two differential 55–70-GHz signals. An STD balun (XF1, see Fig. 14) generates differential signals for the input of the QG. To improve the differential balance of the input LO signals, two sets of buffers (BUF_A and BUF_B) are added between the STD and the QG. Another set of linear buffers (BUF_C_1 and BUF_C_2) are added after the QG to improve the voltage swing before driving the passive mixer (Mixer_1 and Mixer_2). Baseband linear amplifiers are connected after the mixers and drive a 50-Ω port impedance on board with a simulated −3-dB BW of 10–500 MHz. Monte Carlo mismatch simulation results show the worst case IQ amplitude and phase imbalance introduced by the buffers, amplifiers, and mixers to be 0.1 dB and 0.2°, respectively, which is negligible compared to what is introduced by the QG. In addition, any unexpected phase imbalance introduced by the test circuitry may be compensated for the PPF tuning circuit.

VI. Measurement Results

This chip was fabricated in a 28-nm seven-metal layer CMOS process, with an available UTM layer and occupied 0.936 mm × 1.013 mm, including the bond pads. The core two-stage PPF with the feedback control is compact, and occupies an area of less than 20 μm × 40 μm. The die is assembled with the testboard using chip-on-board packaging. A die photograph is shown in Fig. 15.

To test the validity of the proposed QG design, the chip was characterized using Cascade 12000AP Summit on-wafer probe station. Most measurements were performed using an Agilent N5247A PNA-X network analyzer and Agilent 25-GHz BW DSA-X 92504A signal analyzer.

The measurement setup is shown in Fig. 16. In the measurements, 55–70-GHz RF/LO signals were provided by an Agilent network analyzer N5247A and performed using on-wafer probing. All of the lower frequency signals, including the baseband output and dc supplies, were routed to the chip, using a chip-on-board packaging strategy. The entire testboard

TABLE I
COMPARISON TABLE

	JSSC '05 [32]	JSSC '09 [33]	TMTT '12 [34]	This Work	
				TT Wafer	SS Wafer
Architecture	Branch Line Coupler	Distributed Microstrip Shunt-Stubs	Quadrature All-Pass Filter	Two-Stage PPFs with Triode-Region Transistor and FB Control	
Frequency (GHz)	57-64	55-65	55-78.5	55-70[f]	
Phase Imbalance (°)	<15	<5	<9.5	<2[f]	<2.2[f]
Amp. Imbalance (dB)	<1	<1.5	<0.5	<0.32[f]	<0.55[f]
Insertion Loss (dB)	-x-	2.5/4	>3dB[c]	3.5dB[b]	3.9dB[b]
Input Impedance	-x-	-x-	40 Ohm // -x-	150 Ohm // 18fF[a]	155 Ohm // 17fF[a]
Area (um^2)	-x-	-x-	-x-	20×40[d]	
Power Consumption	0	0	0	127-162μW[e]	132-192μW[e]
Process	0.12μm SiGe	90nm CMOS	0.13μm SiGe	28nm CMOS	

[a] Extracted simulation results. [b] Extracted simulation results without real loading from the following buffer stage.
[c] Calculated from the ideal amplitude response of QAF with $\frac{R_s}{R} = 1$.
[d] Area doesn't include the operational amplifier. [e] Power consumption includes the opamp, which has 40μA from a 1.8V supply. The power doesn't include a 6mW LO buffer to drive the proposed quadrature generator.
[f] The reported quadrature mismatch was obtained by fixing I_{Ctrl} every 7GHz.

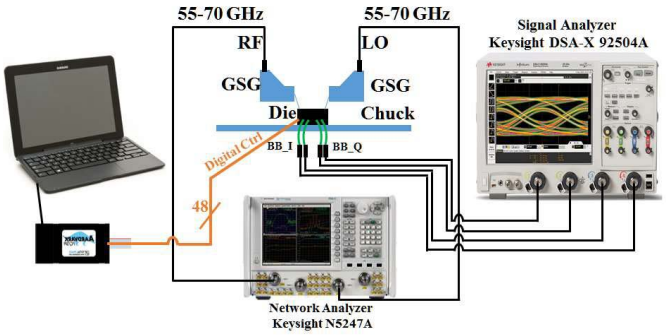

Fig. 16. Proposed IQ generation chip laboratory measurement setup.

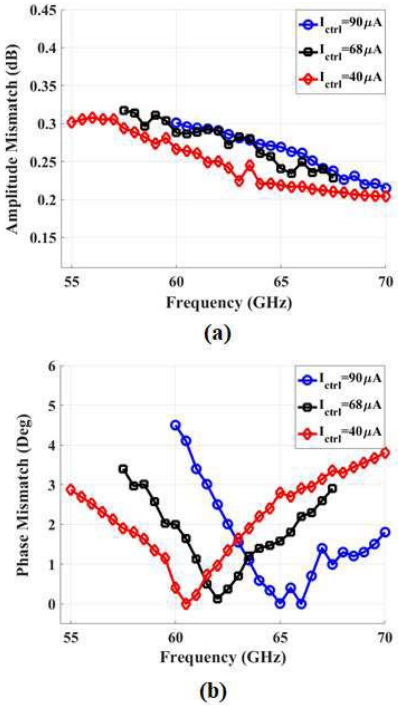

Fig. 17. Measured amplitude/phase mismatch of the proposed tunable IQ generator versus frequency for several values of I_{ctrl}. (a) Amplitude mismatch. (b) Phase mismatch.

was mounted on a custom chuck on the probe station, to allow chip probing of a device mounted on a PCB. The Agilent 25-GHz BW DSA-X 92504A signal analyzer was connected to the baseband output and measured the IQ imbalance in both the time and frequency domains. A laptop with an Aardvark I2C/SPI host adapter (Total Phase Inc.) provided digital control. Measurements were taken with five boards with three of the five assembled with TT die, while the other two were mounted with SS die. FF die is not available for testing.

Using the TT die, both the phase and gain error were measured and plotted versus frequency using several control currents (I_{Ctrl}) values from 40 to 90 μA, which ultimately modulates the triode-region resistors in the PPF; see results in Fig. 17. A worst case measured phase/amplitude imbalance of 2°/0.32 dB (TT dies) and 2.2°/0.55 dB (SS dies) is reported over 7-GHz BW for a fixed value of I_{Ctrl} (see Fig. 18). When I_{Ctrl} is retuned at every 7 GHz, this QG would maintain the measured quadrature error from 55 to 70 GHz (Fig. 17). As mentioned earlier, a bandgap reference supplies the tuning current I_{Ctrl} with sufficient range to maintain the phase imbalance to less than 2° over 7-GHz BW which is compliant with the 802.11ad standard. It is worth mentioning that a fixed resistance given by $V_{\text{RBIAS}}/I_{\text{Ctrl}}$ may not perfectly match the optimum resistance that gives a minimum quadrature phase error, over all PVT (see Fig. 17). The additional parasitic capacitance (see Section IV-C) associated with the triode-region transistor will shift the center frequency of the PPF. In the actual system, a lookup table will tell which control current should be used to cover the desired BW.

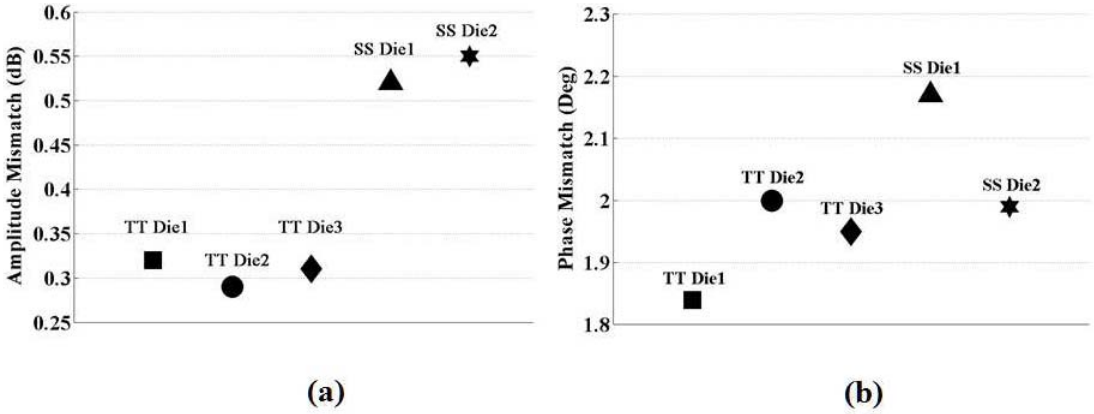

Fig. 18. Measured worst case amplitude/phase mismatch for several available chips. (a) Amplitude mismatch. (b) Phase mismatch.

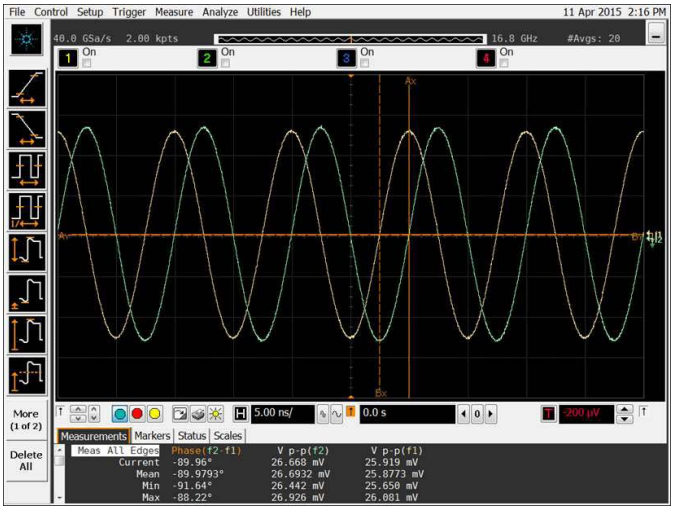

Fig. 19. Baseband quadrature output waveforms measured using oscilloscope. $f_{RF} = 65$ GHz, $f_{LO} = 64.9$ GHz, $f_{IF} = 100$ MHz, $V_{RBIAS} = 100$ mV, and $I_{Ctrl} = 90$ μA.

A screen capture from an oscilloscope is shown in Fig. 19, for a typical signal supplied by the IQ generator. This measurement was taken with a TT die at $f_{RF} = 65$ GHz and $f_{LO} = 64.9$ GHz, and the control voltage/current is 100 mV/90 μA, respectively.

The proposed QG consumes less than 192 μW, of which 120 μA comes from a 1-V supply for the control current of the feedback circuitry and 40 μA from a 1.8-V supply for the opamp. An LO buffer which consumes 6 mA from a 1-V supply drives the QG input impedance which is simulated to be 150 Ω in-parallel with 18 fF.

Several sets of measurements were taken to explore the variation in the IQ imbalance using all five available chips. Fig. 18 shows the measured worst case amplitude/phase mismatch between five different prototype devices. Both TT and SS die give similar phase mismatch results; however, the SS chips exhibit a 0.2 dB greater amplitude mismatch. The increased amplitude mismatch could be the result of a mismatch between the I and Q channels at baseband, i.e., baseband amps in Fig. 14. This process-dependent offset could be mitigated with the use of larger transistor sizes for the buffers and amplifiers in the measurement signal path. In the actual system, the amplitude imbalance in the LO signal path has less impact on the RX EVM performance as compared to the phase imbalance. The switching activity in the mixer, especially passive mixer, reduces the impact of the LO I/Q amplitude mismatch. A detailed circuit performance comparison with other state-of-the-art IQ generators is given in Table I.

VII. Conclusion

A feedback-controlled PPF-based method to generate accurate wideband high-frequency IQ generation is described. A prototype chip is designed with a measured IQ imbalance of less than 2°/0.32 dB (TT dies) and 2.2°/0.55 dB (SS dies) in increments of BW 7-GHz wide, with an overall coverage from 55 to 70 GHz with retuning control currents (I_{Ctrl}).

Potential applications for this technique include 60-GHz transceivers, mm-wave wideband systems, and any radios requiring a wideband low-power highly accurate quadrature generation function.

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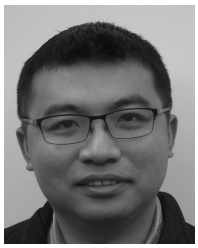

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